ECE 154A Introduction to Computer Architecture
Fall 2012

Dmitri Strukov
<table>
<thead>
<tr>
<th>Instructor</th>
<th>Email</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dmitri Strukov</td>
<td><a href="mailto:strukov@ece.ucsb.edu">strukov@ece.ucsb.edu</a></td>
</tr>
<tr>
<td><strong>Office:</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Office hours:</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HFH 5153</td>
</tr>
<tr>
<td></td>
<td>Tuesday</td>
</tr>
<tr>
<td></td>
<td>10:00 – noon (right after class) or by appointment</td>
</tr>
</tbody>
</table>
Course Logistics : TAs

Junkai Jiang  
Office hours:  
Discussion session:  

Xiang Qiu  
Office hours:  
Discussion session:  

Farnood  
Office hours:  
Discussion session:
Course Logistics: Textbooks


- **Additional (not required)**: The C Programming Language, Kernighan and Ritchie (K&R), 2nd edition

- C language manual webpage from Stanford University
# Course Logistics: Grading (tentative)

- Homework Assignments: 15%
- Projects: 25%
- Quiz 1: 15%
- Quiz 2: 15%
- Final: 30%

---

**Bonus points**
- Class Participation: 5%
- Class Attendance: 5%

No curving
Course Logistics: Approximate Schedule

• Approximate schedule on class syllabus
  – 1 hw/project/quiz per week
  – Hw/projects due one week after assignment in HFH, 3rd floor (box labeled ECE154A)

• Hw, projects description, and solutions will be posted on the web
Layers of Abstractions

Computation is implemented using many layers of abstractions – WHY?
Below the Program

```plaintext
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

```
lw $t0, 0($2)
lw $t1, 4($2)
sw $t1, 0($2)
sw $t0, 4($2)
```
The lowest layer of hierarchy
Major computing platforms

- Application Specific Integrated Circuit
- Field Programmable Gate Array
- Microprocessor

Density, speed vs. Flexibility
Moore’s Law

Predicts: 2X Transistors / chip every 2 years

en.wikipedia.org/wiki/Moore's_law
Technology Scaling Road Map (ITRS)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature size (nm)</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>Intg. Capacity (BT)</td>
<td>2</td>
<td>4</td>
<td>6</td>
<td>16</td>
<td>32</td>
</tr>
</tbody>
</table>

- Fun facts about 45nm transistors
  - 30 million can fit on the head of a pin
  - You could fit more than 2,000 across the width of a human hair
  - If car prices had fallen at the same rate as the price of a single transistor has since 1968, a new car today would cost about 1 cent
Big Ideas

**ASIC**
- computation: custom circuit
- cons and pros: dense and fast but customized to specific computation
- typical use: custom operations repeated many times over time

**FPGA**
- computation: custom circuit on programmable fabric
- cons and pros: middle ground between ASIC and uP
- typical use: custom operations repeated many times over time which are allowed to slowly change over time

**uP**
- computation: sequence of steps (instruction) executed with multifunction blocks
- cons and pros: least dense and fast but very flexible and ubiquitous
- typical use: time varying computations

Because of limited chip real estate uP was the only choice in early days
Plenty resources today → economics define the best computing platform