

# Superconductor Electronics Technology for High End Computing

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**Abstract**— We describe an ongoing program to develop and demonstrate ultra-high performance SFQ VLSI technology to enable superconducting processors for petaFLOPS-scale computing. The computational engines to power petaFLOPS machines at affordable power will consist of 4,096 SFQ multi-chip processors, with 50 to 100 GHz clock frequency and associated cryogenic RAM, operating under a multi-threaded architecture. We are completing FLUX-1, the demonstration of an 8-bit microprocessor chip (5 K gates, 20 GHz clock) and designing FLUX-2, a 32-bit floating-point multiplier with vector register memory. The following stage will be SuperPro, an SFQ multi-processor machine. We discuss the superconducting technology requirements, progress to date, and plan to meet these requirements. We have improved SFQ Nb VLSI by two generations (to a 8 kA/cm<sup>2</sup>, 1.25 μm junction process) and incorporated new CAD tools into our methodology. We have demonstrated methods for recycling the bias current and communication, via flux quanta, at speeds up to 60 Gb/s both on-chip and between chips through a passive substrate. Important challenges include reducing chip supply current and on-chip power dissipation, developing at least 64 Kbit, sub-nanosecond cryogenic random access memory chips, thermally and electrically efficient high data rate cryogenic-to-ambient input/output technology, and advanced Nb VLSI to increase gate density.

## I. INTRODUCTION

THE HTMT (Hybrid Technology Multi-Threaded) architecture study [1] identified SFQ processors as a solution to high-end computing at affordable power because of their inherent ultra-low power and high speed. The baseline design requires 4096 SFQ processors operating at 50 - 100 GHz clock frequency. Since this technology is not yet available "off-the-shelf", a collaborative technology development project was initiated to mature SFQ technology and validate its readiness for a high-end computer. The multi-organization FLUX project has several facets. This presentation discusses the requirements and plans, progress and status, and remaining challenges to achieve and demonstrate the desired maturity.

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## II. REQUIREMENTS AND PLANS

In order to produce the SFQ processors required for a high-end (petaFLOPS) computer, we need a Nb VLSI process [2] based on 20 kA/cm<sup>2</sup>, 0.8 μm junctions with global planarization to support at least six Nb wiring layers. Additionally, we need an advanced gate library, automated CAD tools, 6-inch multi-layer MCM's, at least 64 Kbit, < 1 ns cryogenic RAM chips, high data rate inter-chip communications, cryogenic network switches, and efficient I/O for power and data.

We plan to provide the following key technologies:

- High yield, high density, high speed Nb VLSI.
- Advanced CAD tools.
- Efficient gate libraries.
- Processor architectures.
- Flip-chip packaging.
- High speed inter-chip data transfer.
- Electrically and thermally efficient I/O.

We will demonstrate progress in these key technologies by a succession of increasingly more ambitious SFQ processors. Fig. 1 illustrates the major steps expected in this process. We used a series of technology chips to validate the 4-kA/cm<sup>2</sup> VLSI technology, establish high serial-data-rate inter-chip communications, and develop FLUX-1. We are now developing FLUX-2, a 32-bit floating-point multiplier with vector register memory. FLUX-2 chips will be fabricated in

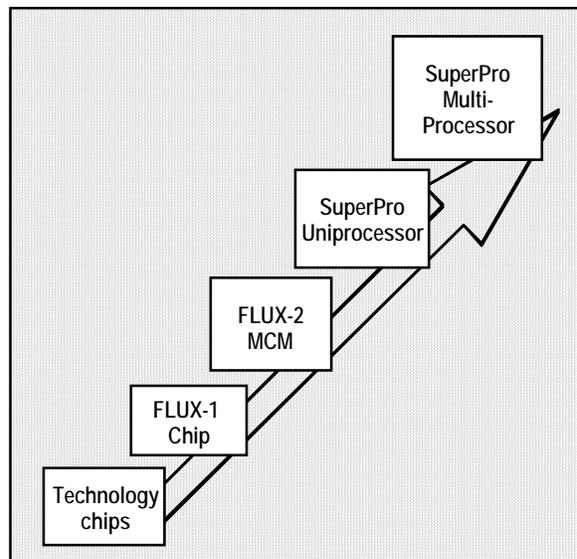


Fig. 1 SFQ Processor Demonstrations Sequence

the present 8-kA/cm<sup>2</sup> VLSI process [2]. The final technology stage will be SuperPro, an SFQ multi-processor, probably configured as a special purpose machine.

The VLSI roadmap is as illustrated in Table I. Its goals are to increase circuit speed and gate density. The principal improvements will be to increase  $j_c$ , reduce junction size, and introduce planarization.

Table I.  
Nb VLSI Technology Roadmap

	1998	2001	Now	+3yrs	+6yrs
Min feature size (μm)	1.5	1.0	1.0	0.6	0.5
Junction size (μm)	2.5	1.75	1.25	0.8	0.5
Junction $j_c$ (kA/cm <sup>2</sup> )	2	4	8	20	50
Kgates per chip	1	5	20	100	500
Chip size (mm <sup>2</sup> )	100	140	100	200	400
No. of Nb levels	4	4	4	5-6	7
No. of resistor levels	2	2	2	2	2
Planarization	No	No	Partial	Yes	Yes
No. of I/O's	128		200		

### III. PROGRESS AND STATUS

First, we established the 4-kA/cm<sup>2</sup> VLSI technology in a series of elementary technology chips. Next, we demonstrated high serial-data-rate inter-chip communications by an efficient, novel flux quantum transmitter and receiver [3]. Next we developed the FLUX-1 chip [4], an 8-bit, single-chip, SFQ microprocessor [5] (equivalent to 5 Kgates) with a 20 GHz clock in 4-kA/cm<sup>2</sup> Nb VLSI process (Fig. 2). We are now designing FLUX-2, a 32-bit floating-point multiplier with vector-register memory. This will be a multi-chip demonstration, including inter-chip data transfer at the clock frequency (Fig. 3). The vector-register chip will be a 4 Kbit serial shift-register operating as a FIFO [6]. The architecture of the floating-point multiplier is in development.

Since the start of this collaborative project in Feb. 2000, we have successfully advanced the technology as follows:

- Improved SFQ Nb VLSI by two generations, from 2-kA/cm<sup>2</sup> to a 8-kA/cm<sup>2</sup>, 1.25-μm junction process.
- Developed on-chip SFQ data transmission through

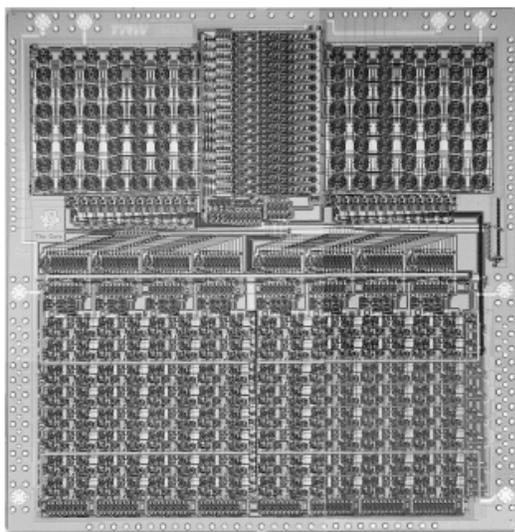


Fig. 2 Photograph of FLUX-1 Chip

striplines [4].

- Demonstrated inter-chip, flux-quantum, serial-data transmission up to 60 Gb/s through passive substrates [3].
- Produced the FLUX-1 microprocessor chip [4].
- Reduced on-chip power dissipation [4].
- Demonstrated methods for re-using the bias current [7].
- Incorporated new design tools into our methodology to improve design success.

### IV. TECHNICAL CHALLENGES

Important technology challenges remain to be addressed.

1. Continue to improve Nb VLSI according to Table I. The major challenge is establishing a fully planarized process.
2. Reduce chip supply current by a factor of 100. Although SFQ circuits have low power dissipation, the bias current will be unacceptably high for high gate count chips.
3. Reduce on-chip power dissipation to its irreducible minimum.
4. Demonstrate at least 64-Kbit, 0.1-ns cryogenic RAM chips. Candidates include hybrid CMOS-SFQ and all-SFQ arrays.
5. Develop thermally and electrically efficient, high-data-rate cryogenic-to-ambient I/O technology.
6. Improve VLSI foundry to increase clock frequency and gate density.

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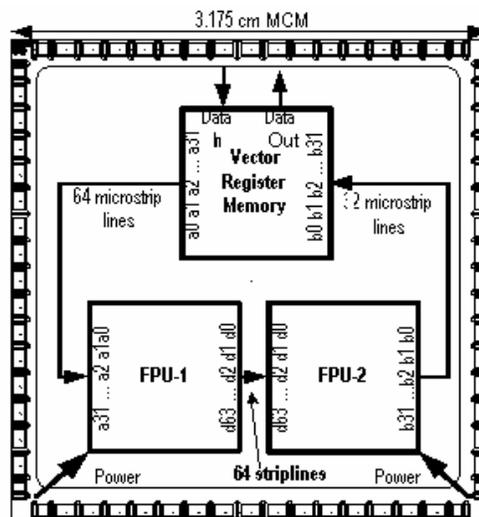


Fig. 3 FLUX-2 Floor-Plan: 3-Chip Floating Point Multiplier

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