CMOL Technology Development Roadmap

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Abstract

We present a preliminary analysis of various options and strategies for the development of hybrid CMOS/nanodevice integrated circuits, in particular those of "CMOL" type and its later varieties, and an assessment of the possible impact of this technology for several key areas of microelectronics. We believe that CMOL technology and/or its cousins is the most natural (and possibly the only practicable) way to extend the exponential (Moore's-Law) development of integrated semiconductor circuits to the next 10 to 15 years, i.e. well beyond the 10-nm frontier.

1. Introduction

The exponential ("Moore's-Law") progress of semiconductor digital integrated circuits [1] has enabled all the current information technology revolution. However, it is generally accepted now that this progress will turn into a crawl some time during the next decade. The most fundamental reason of this anticipated crisis is that the workhorse device of these circuits, the silicon field-effect transistor, requires an accurate lithographic definition of several dimensions including the length and width of its conducting channel. Unfortunately, candid estimates show [2] that alternative electronic devices either run into similar fabrication problems, or have lower functionality, or both.

However, recent experimental and theoretical research results (for reviews, see, e.g., Refs. 2-8) indicate at least one plausible means to avoid the impending crisis: hybrid semiconductor/nanodevice circuits in which a silicon chip is augmented by a top layer of simple (two-terminal) but very small nanodevices with the functionality of programmable diodes. The main idea of this combination is that the two-terminal devices have only one critical dimension (distance between two electrodes) which can be readily controlled, with sub-nanometer precision and without overly expensive equipment, by film thickness.

Figure 1a shows the topology which is the main focus of the current research work in this field: similar nanodevices are formed at each crosspoint of a nanowire crossbar. The advantage of this configuration (in a rudimentary form, suggested in Ref. 9) is that it does not require alignment between the two nanowire levels, and hence may be fabricated by prospective patterning techniques such as nanoimprint. This technique has already allowed to demonstrate a 1,000-device crossbar with a half-pitch F_{nano} of 17-nm [10] and 15-nm ([11], see Fig. 1b), with good prospects for F_{nano} to be scaled down to a few nanometers – see below.

In order to be used effectively, the crossbar needs to be interfaced to the CMOS subsystem in a way which would allow individual access to each crosspoint nanodevice. Several sophisticated techniques based on stochastic doping of semiconductor nanowires had been suggested for this purpose (see Ref. 6 for their critical review); however, the "CMOL" interface [2, 4, 6, 7, 12] seems more general and much easier for the practical implementation. In this approach (Fig. 2) the silicon/nanowire interface is provided by sharp-tip, conical vias ("pins") which are distributed all over the circuit area. The main invention here was a rotation of the nanowire crossbar relative to the rectangular grid of pins (Fig. 2b) by a certain angle. A straightforward inspection of this picture makes it evident that this interface allows the CMOS subsystem to contact each and every nanowire and hence address each individual nanodevice.

Even more remarkably, nanoscale alignment of the crossbar with the CMOS stack is not required for high fabrication yield. (This is only true for the advanced version of the interface, suggested in Ref. 12 and shown in Fig. 2). This fact allows for such advanced patterning techniques as nanoimprint [13] and EUV interference lithography [14] to be used for nanowire crossbar fabrication. Indeed, these techniques do not offer layer alignment comparable in accuracy with their resolution. (This is the reason why these methods

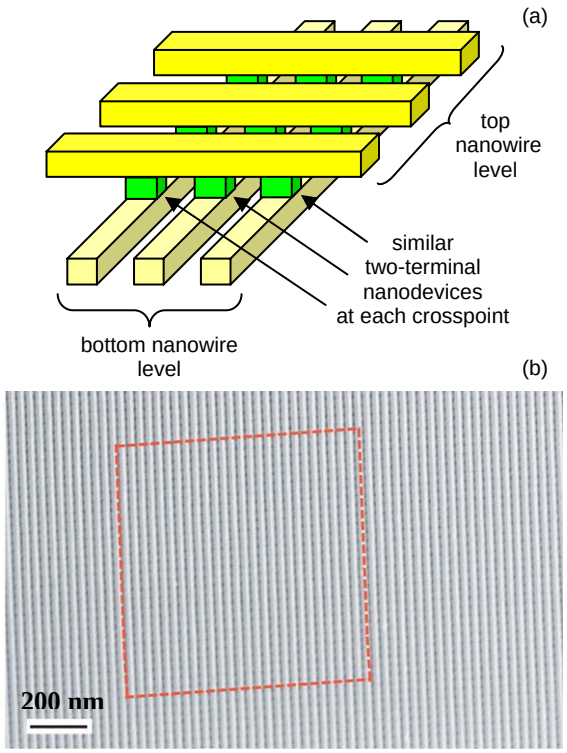

Fig. 1. Nanowire crossbar with two-terminal crosspoint devices: (a) structure (schematically) and (b) an experimental sample with F_{nano} = 15 nm [11].

can hardly be used for further scaling of purely CMOS circuits.)

The other necessary components of the CMOL interface, nanometer-sharp pins, have been repeatedly demonstrated in the context of electron field-emission arrays – see, e.g., Ref. 15.

Finally, recently there was a remarkable progress in fabrication of crosspoint devices with the necessary functionality of "latching switches" (Fig. 3a), notably by Spansion LLC ([16], Fig. 3b) and an IBM-led collaboration [17]. As a result, all major components of CMOL circuits may be considered demonstrated and ready for the beginning of a serious integration work.

On the other hand, recent detailed studies [6, 12] have shown that if the crosspoint devices feature the functionality of programmable diodes, the hybrid circuits may enable (at least) the following applications:

(i) terabit-scale resistive memories with access time below 100 ns and defect tolerance up to 10% [18],

(ii) FPGA-like reconfigurable logic circuits with the area-by-delay product at least two orders of

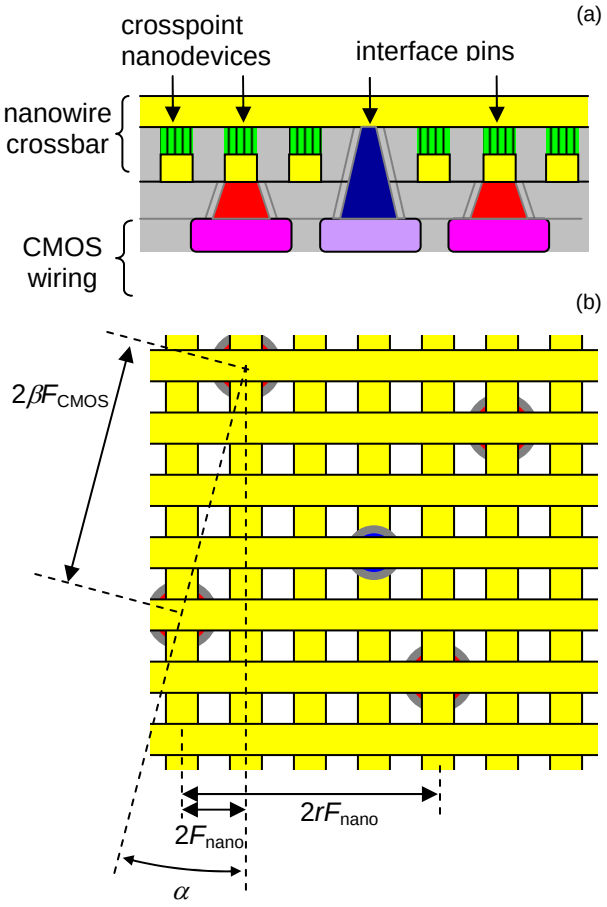

Fig. 2. Area-distributed "CMOL" interface between the CMOS and nano subsystems: (a) side and (b) top view.

magnitude lower than that of CMOS FPGAs fabricated with similar design rules and power per unit area [12, 19, 20, 21], and

(iii) mixed-signal neuromorphic networks ("CrossNets") [22] which may provide unparalleled performance for some important information processing tasks including ultrafast image recognition [23, 24], and in future may become the first hardware basis for challenging the human cerebral cortex in both density and speed, at manageable power [22].

As a result, practical demonstration of first CMOL circuits seems an urgent task which may have serious implications for microelectronics. The goal of this report is to discuss the most important challenges on this way and options for meeting them. In the Section 2, we discuss the main new components of CMOL integrated circuits. Based on this discussion, in Sec. 3 we give a rough estimate for the timeline of the possible progress of CMOL technology and its key applications. Finally, in Sec. 4 we give a very brief summary of our conclusions.

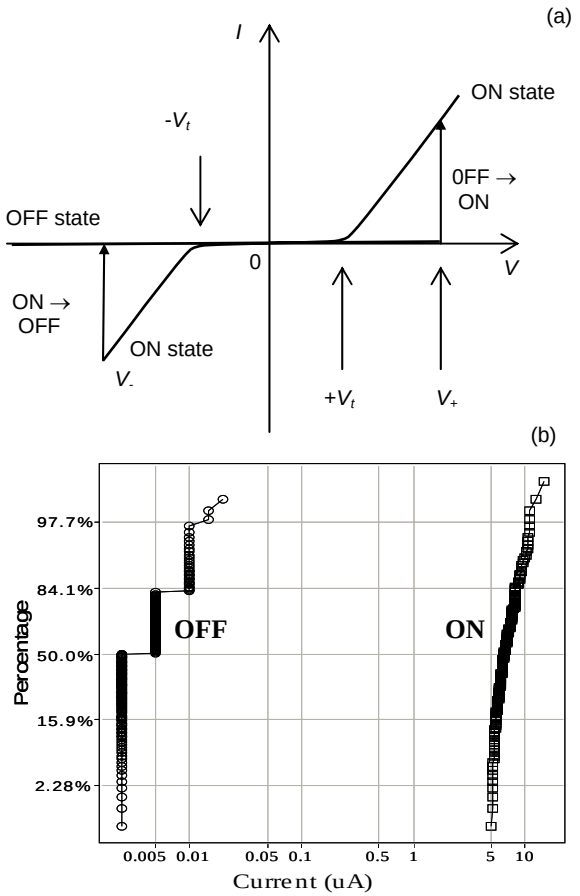

Fig. 3. Two-terminal, bistable crosspoint devices ("latching switches"): (a) *I-V* curve (schematically), and (b) histogram of ON and OFF currents of CuO_x switches [17].

2. CMOL components

Table 1 lists the key parameters and metrics of CMOL circuits, and explains our methodology of determining the values of these parameters in our projections.

2.1. Nanowire crossbars

The very concept of hybrid CMOS/nanodevice circuits is based on the premise of freeing advanced lithographies from the requirement of nanoscale layer alignment ("overlay"). We believe that this "liberation" may allow the advanced lithographies to progress much faster.

Presently, there are two basic options for the formation of crossbar nanowires: nanoimprint lithography (for a recent review see Ref. 13) and EUV interference lithography (see, e.g., Ref. 14). Presently, the former of these techniques is more ready for applications; in particular it has been used for the recent experimental demonstrations of nanowire crossbars [10, 11]. Some results (in particular, the reproducibility of nanometer -scale notches left by the master stamp on several sequential prints) indicate that this technology may be scalable down to ~8-10 nm.

On the other hand, the EUV interference lithography, which does not require stamps, may be more suitable for going beyond the 10-nm frontier, especially taking into account the current industrial effort to develop EUV techniques. Though this effort may never be practicable for the usual lithography, due to the prohibitively expensive reflective optics, it may pay back nicely in the interference lithography where neither the optics nor special masks are needed. (In this approach, parallel nanowires of each level are formed by transfer of an interference pattern of two plane waves of the EUV radiation.) We see no reasons to think that this method cannot be extended all the way down to a few-nm wire width, where CMOL progress may be stopped by a strong growth of wire resistivity ρ, due to strong scattering on the nanowire surface and metallic grain boundaries. (Theoretically, the last limitation might be removed by using single-wall carbon nanotubes or other nanowires. However, so far no practical ways of precise placement of prefabricated nanowires on an integrated circuit surface have been developed, or even rationally envisioned, so we do not consider this option.)

2.2. Crosspoint devices

In essentially all crossbar nanoelectronic circuit architectures developed so far, crosspoint devices are assumed to have the "programmable diode" (a.k.a. "latching switch") functionality – see Fig. 3a. At low applied voltage, such device operates as a diode, i.e. has a nonlinear monotonic *I-V* curve, but high voltage may switch it from this "ON" state into the virtually nonconductive "OFF" state and back. This means, in particular, that the device may operate as a memory cell storing one bit of information in its internal state.

Several groups demonstrated devices with this functionality using layers of various material, oxides of several metals (see, e.g, Ref. 16), relatively thick organic films both with and without embedded metallic clusters, self-assembled molecular monolayers, and chalcogenide films -see, e.g., Ref. 17. (See Ref. 18 for a review of the recent work in this direction). The excellent reproducibility of the copper oxide devices, demonstrated by Spansion LLC [16], is especially spectacular – see Fig. 3b.

Table 1. CMOL technology parameters

##	Notation	Parameter	Definition/Comments
1	F_{CMOS}	CMOS wiring half-pitch	As produced by the usual patterning
2	F_{nano}	Nanowire half-pitch	As produced by advanced patterning
3	n	Crosspoint device ("function") density	$n = 1/(2F_{nano})^2$
4	β_{min}	Interface pin mesh size in the units of $2F_{CMOS}$	See note [(a)]
5	r	Main topological parameter (integer, Fig. 2a)	r = ceil $[(\beta_{min}F_{CMOS}/F_{nano})^2-1]^{1/2}$ [(b)]
6	α	CMOL interface rotation angle (Fig. 2a)	α = arctan $(1/r)$
7	L	Nanowire segment length (excluding the gap)	$L = 2r^2F_{nano} \approx (2\beta F_{CMOS})^2/2F_{nano}$ [(c)]
8	N	Number of crosspoint nanodevices per segment	$N = r^2 = L/2F_{nano}$ [(d)]
9	ρ	Nanowire resistivity	Affected by nanowire width F_{nano} [(e)]
10	R_W	Nanowire segment resistance	$R_W = \rho_{ef}L/(F_{nano})^2$
11	C_0	Nanowire capacitance per unit length	See note [(f)]
12	C_W	Nanowire segment capacitance	$C_W = C_0L$
13	V_{DD}	Power supply voltage	For logic circuits, optimized value [19]
14	P_0	Average power per unit area	Including static and dynamic power
15	f	CMOL clock frequency scale	$f = 4P_0(\beta F_{CMOS})^2/(V_{DD})^2C_0L$ [(g)]
16	q	Bad nanodevice fraction	Affects fabrication yield [(h)]

[(a)] $2\beta F_{CMOS}$ (see Fig. 2a) is the distance between adjacent interface pins leading to one layer of crossbar nanowires, and is essentially the linear size of the smallest useful CMOS cell serving one input and one output nanowire fragments. For a CMOL memory cell, β_{min} has been estimated as 1.6 [18]. However, in the estimates below we will accept a more conservative value $\beta_{min} = 4$, reflecting the fact that the back-end (top layer) wiring in CMOS circuits is substantially more crude that that their front end (lower layers) for which F_{CMOS} is traditionally cited.

[(b)] Integer r defines the CMOL interface tilt angle α = arctan $(1/r)$ - see Fig. 2. For each given F_{CMOS}/F_{nano} ratio, it should be determined as the smallest integer satisfying the requirement $\sin\alpha \equiv (1 + r^2)^{-1/2} < F_{nano}/\beta_{min}F_{CMOS}$. For relatively large values of the F_{CMOS}/F_{nano} ratio, $r \approx 1/\alpha \approx \beta_{min}F_{CMOS}/F_{nano}$.

[(c)] Interface pins going to the top crossbar level, intentionally interrupt the lower level nanowires – see Fig. 2. Thus the latter wires are naturally divided into segments of length L, but they (as well as the top layer wires) may certainly be divided into smaller segments if necessary.

[(d)] N is an important parameter because it shows how many crosspoint devices are connected to one interface pin of a CMOS cell. Since each device leads to another pin, N may be also understood as the connectivity of CMOS cells.

[(e)] The resistivity may be crudely estimated as $\rho_{ef} \approx \rho_{ph}(1+ L_{ph}/F_{nano})$, where ρ_{ph} is the table value for the metal resistivity (determined by electron-phonon scattering) and L_{ph} is the corresponding mean free path of an electron – for good metals of the order of 30 nm. The exact value of ρ_{ef} not very important, because estimates show that for good metals the nanowire segment resistance R_W (see line 10 of the Table) is substantially lower than the minimum, power-determined values R_{ON} of the crosspoint devices. On the other hand, the condition $R_W < R_{ON}$ essentially forbids the use of semiconductor or molecular nanowires in these circuits.

[(f)] For this parameter, we are using our calculations of C_0 as a function of F_{nano} and the interlayer spacing t - see Fig. 13 of Ref. 19 – assuming t to be equal 4 nm, and the dielectric constant of the insulator to be 3.9 (SiO_2). The use of low-κ dielectrics would decrease C_0 (and hence increase the circuit speed) correspondingly.

[(g)] This expression results from the requirement for the static power (per unit area) of open crosspoint devices (which is the dominating component in the CMOL power budget [19, 20]), not to exceed P_0 (line 14). The average number of open crosspoint devices per unit area may be estimated as $(i/2)/(2\beta F_{CMOS})^2$, where i is the average CMOL gate fan-in, and the power in open device as $(V_{DD})^2/R_{ON}$. After R_{ON} has been found from the above requirement, f may be estimated as $1/2d(R_{ON}/i)(C_0L)$, where d is the logic pipeline depth, of the order of 10 for most circuits. The result is independent of i.

[(h)] So far, the most detailed evaluations of CMOL circuit defect tolerance have been carried for just one defect type (equivalent to "stuck-on-open" faults) which is believed to be dominant at the initial stage of development of this technology. Only in the very recent work [21] we have estimated the effect of other defects, including "stuck-at-closed" faults and nanowire breaks on CMOL FPGA circuits. The extension of this analysis to other CMOL circuits (including digital ASICs and mixed-signal networks) is an urgent research task.

Table 2a. CMOL circuit parameters: Near-term prospects

Parameters (units)	2009	2010	2011	2012	2013	Comments
Half-pitch F_{CMOS} (nm)	50	45	40	36	32	Follows ITRS until 2013[a]
Half-pitch F_{nano} (nm)	20[b]	18	16	14	12	Mostly nanoimprint + MO_x devices
Nanodevice density n (Giga/cm^2)	63	77	98	128	174	Grows fast
Parameter r	10	10	10	11	11	Barely changes
Connectivity N	100	100	100	121	121	Barely changes
Interface rotation angle α (°)	5.7	5.7	5.7	5.2	5.2	Barely changes
Nanowire segment length L (μm)	4.0	3.6	3.2	2.8	3.0	Decreases slowly
Power supply voltage V_{DD} (V)	0.3	0.3	0.3	0.3	0.3	Almost constant
Maximum power P (W/cm^2)	200	200	200	200	200	Constant
CMOL clock speed scale (GHz)	1.4	1.3	1.1	0.9	0.8	CMOL circuits are not too fast! [d]
Defect fraction q (%)	20	15	10	7	5	Improves fast [e]

Table 2b. CMOL circuit parameters: Long-term prospects

Parameters (units)	2016	2019	2022	2025	2028	Comments
Half-pitch F_{CMOS} (nm)	30	28	26	24	22	Decreases very slowly [a]
Half-pitch F_{nano} (nm)	10	6	4	3.5	3	Mostly EUV + SAM devices
Nanodevice density n (Tera/cm^2)	0.25	0.70	1.0	2.0	2.8	Unprecedented density reached
Parameter r	12	19	26	28	30	Increases substantially
Connectivity N	144	361	676	784	900	Increases fast
Interface rotation angle α (°)	4.8	3.0	2.2	2.0	1.9	Decreases
Nanowire segment length L (μm)	2.8	4.3	5.4	5.4	5.4	Increases slowly
Power supply voltage V_{DD} (V)	0.3	0.3	0.3	0.3	0.3	Almost constant
Maximum power P (W/cm^2)	200	200	200	200	200	Constant [c]
CMOL clock speed scale (GHz)	0.7	0.4	0.3	0.2	0.2	Slower still [d]
Defect fraction q (%)	3	1	0.3	0.1	0.03	Improves slower [e]

[a] We believe that for F_{CMOS} the ITRS [1] gives reasonable predictions for the near-term years, all the way to the 32-nm technology node, but not for the long-term years when the skyrocketing fabrication facilities cost will prevent the further minimum feature shrinkage. (Actually, the ITRS document acknowledges that there are no "known solutions" for that period.) As a result, we assume that the further progress will go at a much slower pace.

[b] Though single samples of crossbars with F_{nano} down to 15 nm have been already demonstrated experimentally [10, 11], their reproducibility still has to be improved substantially for the industrial introduction. This is why we will assume a more conservative starting point: F_{nano}= 20 nm in Year 2008.

[c] For P, we are using the ITRS prediction [1] for high-performance ICs.

[d] A certain decrease in speed is more than compensated by the circuit density growth. There could be several ways, still unexplored quantitatively, to increase the speed even further. One of them is additional partitioning of the nanowire fragments when parameter N becomes larger than necessary for the useful cell connectivity. Such partitioning will cut the nanowire capacitance and hence increase its recharging speed.

[e] We assume a very conservative pace for the device defect reduction. (It factors in the necessity, discussed in Sec. 3, of transfer from metal-oxide devices to SAM-based devices by the end of the first time period.) In the light of the very high defect tolerance of CMOL circuits [18-24], this slow pace does not hinder the anticipated CMOL progress too much.

Table 3a. Some CMOL applications: Near-term prospects [a]

Metrics (units)	2009	2010	2011	2012	2013	Comments
Half-pitch F_{CMOS} (nm)	50	45	40	36	32	See Table 2a above
Half-pitch F_{nano} (nm)	20	18	16	14	12	-"-
CMOS memories (Gbits/cm^2)	6.7	8.2	10.5	13	16	Follows ITRS (with $A = 6F^2_{CMOS}$)
CMOL memories (Gbits/cm^2)	4	10	23	36	67	Initial progress impacted by q [b]
CMOS logic (Mgates/cm^2)	0.4	0.5	0.6	0.8	1.0	Rescaled from 0.18 μm rules [c]
CMOL logic (Mgates/cm^2)	625	775	1,000	1,200	1,500	Speed close to CMOS logic [d]

Table 3b. Some CMOL applications: Long-term prospects [a]

Metrics (units)	2016	2019	2022	2025	2028	Comments
Half-pitch F_{CMOS} (nm)	30	28	26	24	22	See Table 2a above
Half-pitch F_{nano} (nm)	10	6	4	3.5	3	-"-
CMOS memories (Gbits/cm^2)	18	21	25	29	35	Follows A = $6F^2_{CMOS}$
CMOL memories (Gbits/cm^2)	100	350	900	1,200	1,700	Spectacular progress at lower q
CMOS logic (Mgates/cm^2)	1.1	1.3	1.5	1.7	2.1	Rescaled from 0.18 μm rules [c]
CMOL logic (Mgates/cm^2)	1,700	2,000	2,300	2,700	3,200	Speed close to CMOS logic [d]

[a] All the estimates are for the original CMOL architecture rather that for its simplified version [32] or the bonded-chip ("3D") version [33], which were suggested later.

[b] Note the low initial density of CMOL memories, due to the anticipated high number of defective crosspoint devices at the initial stage of the CMOL technology development (see Table 2).

[c] Here the logic gate density is calculated by rescaling the tile area consisting of one 4-input LUT for CMOS FPGAs. These density numbers represent the best case when all CMOS cells are used to implement logic functions (e.g., for circuits which feature very strong systolic-like interconnect). The simulation results of more general representative circuits [12] show that the useful density may be somewhat lower (typically by less than an order of magnitude) due to the allocation of CMOS cell for routing purposes.

[d] See the second line from the bottom in Table 2. Note, however, that for some applications (see, e.g., Ref. 20), CMOL circuits may provide a much higher speed, because they may enable circuits with much shorter interconnects.

For most of these devices, the bistability (memory) mechanism is not yet clear. For the currently most reproducible metal-oxide devices it is probably due to electron trapping in localized states [16], though the ion drift typical for solid-electrolytes cannot be excluded. The basic drawback of devices based on any of these mechanisms is that most of ON current is transferred through percolation trajectories formed between quasi-localized electron states. In order the current density to be reasonable, distance between such localized states cannot be much smaller than ~3 nm. In order to be statistically reproducible, the device should have a large number of the states. This is why the extension of the excellent reproducibility demonstrated for crosspoint devices with $F_{nano} > 100$ nm (as in Ref. 16) to cells with $F_{nano} < 10$ nm may present a major challenge.

This problem may be addressed using uniform self-assembled monolayers (SAM) of specially designed molecules [6, 25] implementing single-electron latching switches [26]. (Metal-based, low-temperature prototypes of such switches, with multi-hour retention times, have been demonstrated experimentally [27]. However, so far molecular implementations have been only demonstrated – see, e.g, Refs. [28, 29] - for the main components of these devices, single-electron transistors.) A major challenge on this way is the reproducibility of the interface between the monolayer and the second (top) metallic electrode, because of the trend of the metallic atoms to diffuse inside the monolayer during the electrode deposition [30]. Recent

very encouraging results towards the solution of this problem have been obtained using an intermediate layer of a conducting polymer [31].

This is why we believe that the first generations of CMOL circuits will be based on metal-oxide junctions, but that by the time (Year 2010 or so) when F_{nano} will be scaled down to ~10 nm, the junctions will be replaced with single-electron-latch-based SAM devices, with other devices (e.g., ones based on chalcogenides [17]) presenting important backup options.

2.3. Interface pins

This is probably the simplest part of CMOL circuitry, but still requires some work. Indeed, the demonstrated conical points with few-nm-sharp pins (see, e.g., Ref. 15) have been based on highly doped silicon or other semiconductors. Since in CMOL the pins have to be implemented on the back end of the CMOS subsystem, using high-quality silicon may be difficult because of the necessity to use low-temperature processes. (High temperature would damage the lower layers of metallic wiring.) Hence it would be beneficial to use metallic rather than silicon pins.

3. Anticipated Development Timeline

Based on the arguments of the previous section, we can make a (very subjective) prediction of the possible development of CMOL fabrication technology- see Tables 2a and 2b. Following the ITRS [1], we are presenting the results separately for two time periods:

- the "near-term" years (2008-2013) may be considered as the initial stage of CMOL technology development, at which this technology will need to coexist with CMOS, and

- the "long-term" years (2013-2028) present the anticipated mature age of CMOL technology when it has taken over the traditional silicon (CMOS) technology for most IC applications.

Plugging the CMOL parameter estimates made in the last section into the results of theoretical analyses [12, 18-24] of CMOL circuits crafted for their main digital applications, one arrives at the estimates shown in Tables 3a and 3b. (The studies of neuromorphic networks for advanced signal processing [22-25], which may eventually become the main application of integrated circuits, are still in infancy, and their impact is very hard to evaluate.)

Possibly the most important disclaimer is that all our time predictions are conditioned by sufficient funding, when the technology's progress is limited by its own learning curve.

4. Discussion

The estimates listed in the tables indicate that the CMOL technology may enable the extension of the exponential progress of microelectronics well beyond the "red brick wall", postponing the Moore's Law demise, crudely, from Year 2013 to Year 2028 or so. Note that these estimates do not take into account possible substantial reserves of that technology, including:

- CMOL circuits using crosspoint devices with negative differential resistance (NDR). According to the recent calculations [34], this effect should take place in virtually all molecular single-electron transistors which can withstand source-drain voltages of the order 1 – 2 volts. This effect may allow signal restoration in the nano subsystem, without diving to CMOS at each logic step, and increase the circuit density significantly [35].

- two-chip ("3D") CMOL circuits [33] which can at least double the circuit density and also simplify the interface fabrication.

Of course, bringing this technology to reality will take a very substantial R&D effort. In our view, the most urgent tasks of the effort include:

- progress of advanced patterning techniques, notably including nanoimprint and EUV interference lithography, in order to improve their resolution;

- experimental demonstration of metallic interface pins;

- development of high-yield fabrication techniques for sub-10-nm crosspoint nanodevices, for example those based on self-assembled monolayers of molecules implementing single-electron latching switches;

- development of better CMOL circuit architectures and tools for their computer-aided design.

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