# Analog-Input Analog-Weight Dot-Product Operation with Ag/a-Si/Pt Memristive Devices

Ligang Gao, Fabien Alibart, and Dmitri B. Strukov*
Department of Electrical and Computer Engineering
University of California Santa Barbara, Santa Barbara, CA 93106, USA
*strukov@ece.ucsb.edu

***Abstract* - We demonstrate that hybrid circuit consisting of Ag/a-Si/Pt memristive devices and silicon operational amplifier can perform analog dot-product computation. The high conductive states in the considered memristive device are linear, making it useful for general analog-input analog-weight operations. In particular, in proposed hybrid circuits, input analog voltage is multiplied by analog weight (conductance) of memristive devices, and the resulting currents are passively summed with the inverting configuration operational amplifier. The proposed concept is checked experimentally by demonstrating passive mixing of two continuous analog signals using a discrete chip operational amplifier and Ag/a-Si/Pt memristive devices, which are programmed using a recently demonstrated variation-tolerant algorithm with a high precision.**

***Index terms: Memristor, Analog computing, Hybrid circuits, Dot-product computation, Conductive bridge memory, RRAM***

## I. INTRODUCTION

Memristors allow for very compact analog nonvolatile memory implementation, which is suitable for a variety of analog circuit applications [1-10]. Let us consider one of the very attractive applications of memristive devices in the analog domain: a circuit performing analog dot-product (multiply-and-add) computation.

Figure 1(a) shows implementation of dot-product operation with hybrid CMOS/memristor circuits [11, 12]. The input voltage is multiplied by the weight (conductance) of memristive device, and the resulting currents are summed on a wire that is virtually grounded with operational amplifier (op-amp). The total current is converted back to voltage by negative feedback op-amp so that the output voltage of the circuit is

$$V_{\text{output}} = - R_{\text{f}} \sum V_{\text{input\_}i} \times 1/R_i \,. \quad (1)$$

Dot-product computation is a typical bottleneck operation in many low-level information processing tasks, such as spatial filtering and feature extraction [12, 13]. It is also the most frequent operation in artificial neural networks and a key part of resistor ladder digital-to-analog converters [12, 14].

The circuit on Fig. 1(a) maps easily onto a one-dimensional crossbar structure (i.e. with one horizontal wire crossing several vertical ones). By adding more horizontal wires with attached memristive devices and op-amps serving it, the circuit is easily generalized to perform matrix operations.

Recently, we have demonstrated a 2-input dot-product operation with hybrid CMOS/memristor circuits [11]. In that work the state of titanium dioxide memristive devices was tuned to high precision by using a variation-tolerant algorithm. Because of nonlinear *I-V* characteristics for ON and OFF states for titanium dioxide memristive devices, their weight [i.e. $1/R_{\text{i}}(V_{\text{input\_i}})$] depends on the applied bias, which restricted us to using only digital-input voltage in the demonstrated dot-product circuits. The purpose of this work is to demonstrate more general analog-input analog-weight dot-product operations implemented with electrochemical Ag/a-Si/Pt memristive devices [15-17]. In particular, we demonstrate that Ag/a-Si/Pt memristive devices can be successfully tuned to a precise resistance state with linear *I-V* in a given range of operation in order to implement the weighting of each input signal. We also study the intrinsic switching noise in memristive devices and its impact on the performance of dot-product circuits.

Electrochemical memristive devices (also known as conductive bridge memory) have been extensively studied in the past few years [18-22]. Application of electrical potential across two terminals in such devices leads to the formation of a conducting filament composed of metallic ions from the reactive electrode. For example, for Ag/a-Si/Pt devices the switching to the ON state (set process) involves electro-oxidation of the Ag electrode and the drift of Ag ions towards an inert (Pt) electrode in a-Si film with subsequent reduction. The resulting filament can be dissolved (reset process) by applying reverse bias polarity. Compared to other electrochemical memristive devices (e.g. to those based on chalcogenide materials), Ag/a-Si/Pt devices have superior properties (e.g. CMOS processing compatibility [23-26]).

## II. EXPERIMENTAL RESULTS

### A. Device Fabrication

The memristive device consists of a top electrode (Ag), the a-Si layer, and Pt as the bottom electrode. An evaporated Ti/Pt

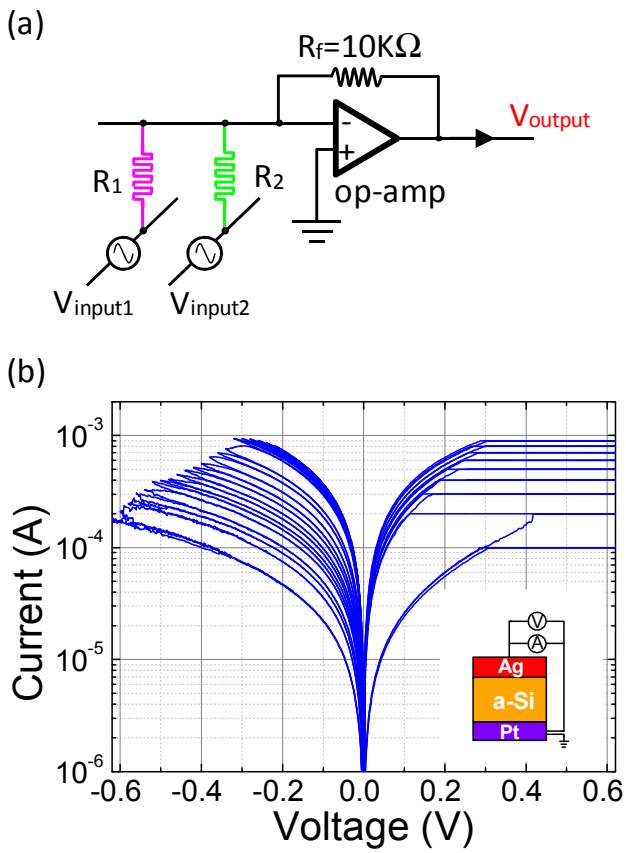


Figure 1. (a) Analog dot-product circuit consisting of the memristive devices and integrated circuit operational amplifier, and (b) *I-V* characteristics of Ag/a-Si/Pt device. The inset shows schematically device structure.

bottom electrode (5nm / 35nm) is patterned by standard optical lithography technique on a $Si/SiO_2$ substrate (500 µm / 200 nm, respectively) at a rate of 0.1 nm/s. A 40 nm a-Si active layer is then deposited by plasma-enhanced chemical vapor deposition at 300°C and a pressure of 600 mT, using $SiH_4$ (2% in He). The orthogonal top electrode is defined by a lift-off step. An Ag/Au electrode (50 nm / 25 nm) is evaporated on top of the a-Si active layer. After deposition, the device was annealed at 450° C in high vacuum condition ($10^{-8}$ T) to diffuse the Ag atom to a-Si film.

### B. Device I-V Characteristics

Multistate memory operation is obtained by controlling the size of a filament(s) during set and reset processes. Figure 1(b) shows typical *I-V* characteristics with multiple resistance states achieved by controlling the sweeping voltage magnitude during reset process (negative polarity), or by controlling the Current Compliance (CC) during the set process (positive polarity). The poor apparent ON/OFF current ratio, in comparison to other devices reported in the literature, is due to the necessity of keeping the device in the ohmic regime throughout the dynamic range. In this particular case, the ohmic *I-V* characteristic of the device implies that the filament bridges two electrodes and that the device's conductivity is controlled by changing the geometry (i.e. diameter and shape) of the filament(s). The resulting dynamic range is determined by a minimum $R_{ON}^{L}$ and maximum $R_{ON}^{H}$ values of resistance for the device in the ON state (i.e. for filament bridging the electrodes). A full OFF state (no filament bridging the electrodes) is achieved by applying voltages less than -1.2 V and results in the ON/OFF current ratio exceeding $10^3$ (not shown in the figure). In this paper we do not program devices to an OFF state, because it results in a weight "0" for dot-product operation. However, it is an important feature of input selection in order to enable/disable a given input.

### C. Switching Dynamics

In order to characterize switching dynamics for Ag/a-Si/Pt devices, pulse protocol measurements are employed [11]. Application of short pulses prevents the devices from overheating and allows for better control of switching, as compared to that of quasi DC sweeping measurements. The latter also typically requires current compliance, which is more challenging to implement in crossbar structures.

Figure 2 shows a more accurate analysis of switching dynamics for the case of tuning the device between $R_{ON}^{L}$ and $R_{ON}^{H}$ states. This measurement is composed of two different pulses:

(i) The write pulses that induce a change in the resistance state ($T_{write}$ = 400 ns); and

(ii) The non-disturbing read pulses ($V_{Read}$ = 0.1 V and $T_{Read}$ = 1 ms).

The analysis of the resistance change as a function of the cumulative time (defined as the summation of all previous write pulses applied to the device during the transition) provides important insight into the analog operation of a memristive device:

(i) The set transition is less controllable, most likely due to positive feedback during ON switching. Shorter pulse duration during writing should circumvent this problem, but this is not achievable in our actual setup, which is limited to 200 ns.

(ii) A better accuracy for tuning devices to a desired state could be achieved with smaller applied voltages. This advantage is balanced by the exponentially longer time needed to reach that state. The tradeoff between tuning time for a certain state and accuracy with which this state can be reached needs further investigation and is beyond the scope of this paper.

### D. Tuning of Memristive State

Earlier we proposed a variation-tolerant algorithm to cope with these two issues [11]. The simple algorithm is based on two sequences of voltage pulses with increasing amplitude. One sequence of pulses is used to implement gradual set, and another one, with opposite polarity, is used for gradual reset switching. In particular, the reset sequence always starts with a -0.3 V voltage pulse, and the amplitude of every new (write) pulse in a sequence is increased by 0.1 V with respect to that of the preceding pulse. The write pulses are alternated with non-disturbing read pulses at $V_{Read}$ = 0.1 V, which are applied to interrogate the current device state. The sequence is stopped

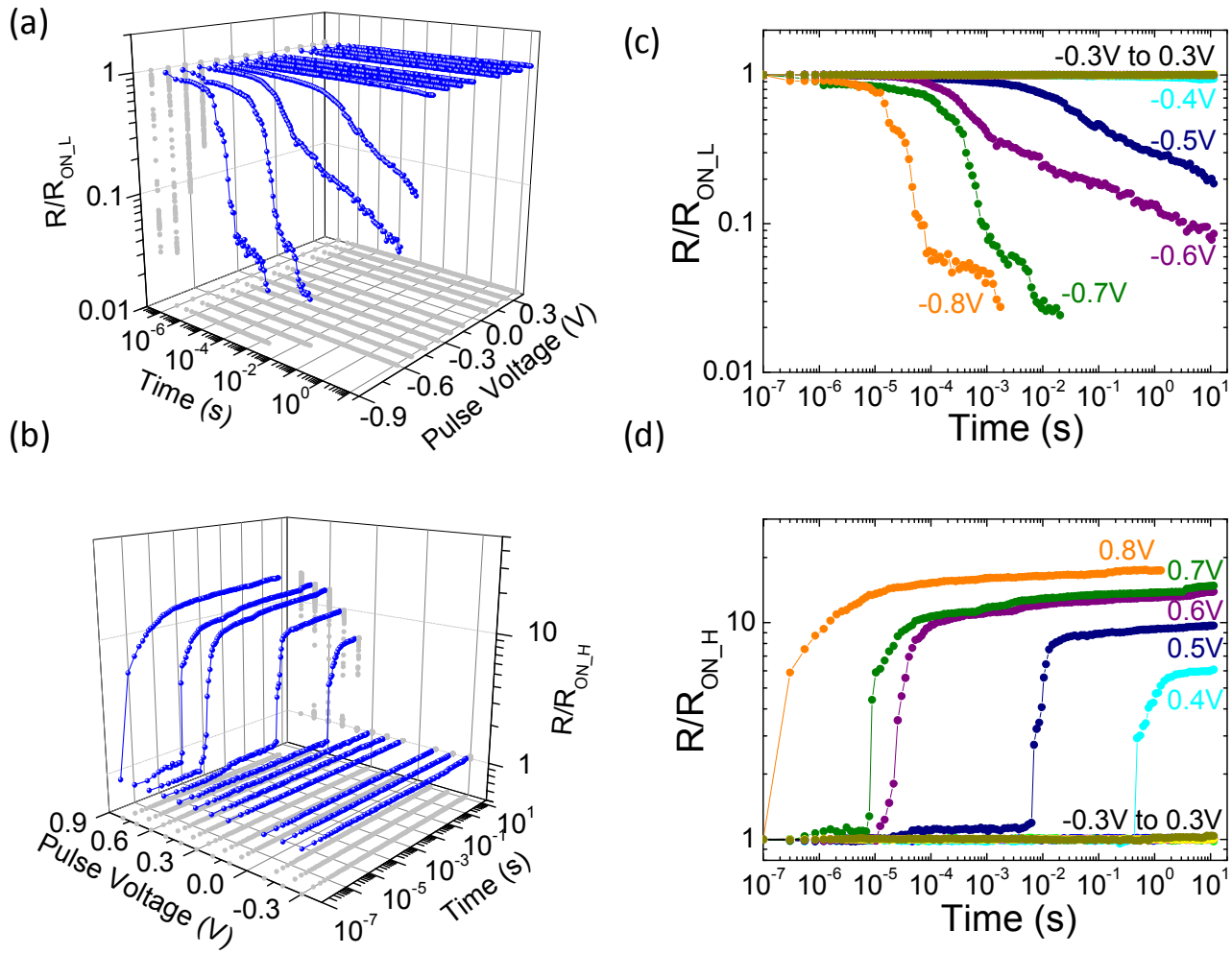


Figure 2. Characterization of switching dynamics in Ag/a-Si/Pt devices. (a) Gradual set and (b) reset of the resistance state is realized by appling external voltage pulses with variable amplitude and duration. Panels (c) and (d) show the same data on 2-D plot for gradual set and reset transitions, respectively.

once read pulse confirms overshooting of the desired resistance state. At this point, if correction is needed, the set sequence is applied with a voltage pulse starting at 0.3 V. While application of several sequences might be needed to converge on a desired state [11], a single gradual reset transition is typically sufficient for the considered devices. Figures 3(c) and (d) present the results of programming devices to different resistance states. These figures also demonstrate that the state is retained for over 3000 s in all cases.

### *E. Dot-Product Circuitry*

Figures 3(a) and (b) show experimental demonstration of analog-input analog-weight dot-product operation with Ag/a-Si/Pt memristive devices, which are tuned to a given resistance state using the described algorithm. The CMOS circuitry was emulated by a breadboard circuit with bipolar op-amp UA741 and $R_f$ = 10 kΩ resistor. Before running the dot-product computation, memristive devices were disconnected from op-amp and tuned to a specific state using a B1500 Agilent parameter analyzer.

In particular, Fig. 3 shows dot-product operation with two continuous AC sinusoidal input signals, with voltage swing = 0.1 V, $f_1$ = 1 KHz and $f_2$ = 5.7 KHz. The amplitude for input signal is small enough that it does not change the resistance state of memristive devices, for which a safe non-disturbing operation is ensured when applied bias is in the range -0.3 V $\leqslant V_{input} \leqslant$ 0.3 V (Figs. 2(a), (b)).

## III. Discussion and Summary

In order to demonstrate scaling of an input signal by memristive device weight, the output signal is post-processed using fast Fourier transform (FFT) analysis. The largest frequency component in the spectrum is proportional to the corresponding weight of the memristive device (Figs. 3(c), (d)). Two following observations can be drawn from this measurement:

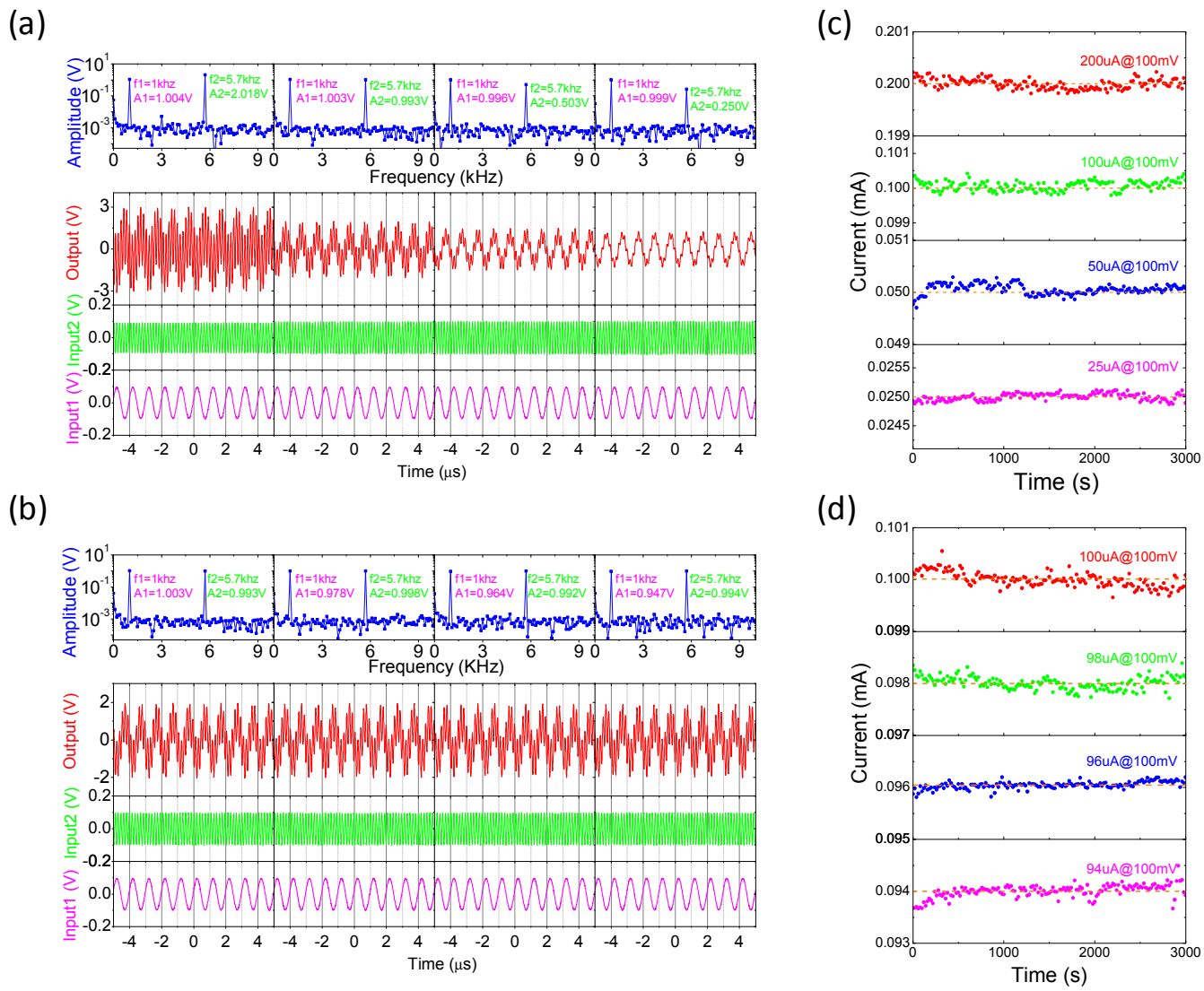


Figure 3. Illustration of analog-input analog-weight continous dot-product operation with silicon operational amplifier and two Ag/a-Si/Pt devices. (a) The device 2 is set with high precision to 200 μA, 100 μA, 50 μA and 25 μA, respectively, while the device 1 is fixed to 200 μA. (b) The device 1 is set with high precision to 100 μA, 98 μA, 96 μA and 94 μA, respectively, while the device 2 is fixed to 200 μA. The top figure for panels a and b shows FFT analysis of output signal. Panels (c) and (d) display current measurements for particular resistance states used in the demonstration.

(i) The dot-product computation can be realized in the full dynamic range of the devices ($R_{ON}^{L}/R_{ON}^{H}$). This dynamic range of operation is the same for all measured devices and is not affected by dispersion between devices.

(ii) The maximum precision for weight tuning using the developed algorithm is close to 1%, which is roughly equivalent to 7-bit accuracy; however, it can be significantly worse for some resistance states.

More specifically, these results reveal one of the main challenges for achieving better tuning accuracy: the intrinsic random telegraph noise (RTN) of memristive devices [27-32]. The cause of such RTN is most likely due to the oscillation of ions in the filament between two traps. The bottom left inset of Fig. 4(b) shows a typical measurement of RTN in our devices where more than two states can be identified. To further quantify the impact of the noise, Fig. 4(a) shows simple RTN analysis for different resistance states. From a power spectrum density analysis (Fig. 4(b)), RTN noise is more severe for the device in a high-resistance state. This leads to an accuracy limitation of about 2.7% for the highest ON resistance state (10 kΩ), as shown in the top-right inset. Though such noise might be a problem for some applications where high accuracy is desired (e.g. digital-to-analog converters), it is probably manageable for the majority of applications, given that analog computing is only practical for low-accuracy analog signals [33].

In summary, we have experimentally demonstrated analog-input analog-weight dot-product computation in a hybrid circuit composed of Ag/a-Si/Pt memristive devices and a silicon operational amplifier, which is a very promising application of memristive devices in the context of information processing. The accuracy for tuning memristive device states was limited to about 3% (of the desired state) in the worst case (i.e. highly resistive states), due to random telegraph noise.

## ACKNOWLEDGMENT

This work is supported by the Air Force Office of Scientific Research (AFOSR) under the MURI grant FA9550-12-1-0038.

## REFERENCES


[1] D. B. Strukov, and H. Kohlstedt, "Resistive switching phenomena in thin films: materials, devices and applications," MRS Bulletin, vol. 37, pp. 108-114, Feb 2012.

[2] S. Shin, K. Kim, and S. M. Kang, "Memristor applications for programmable analog ICs," IEEE Transactions on Nanotechnology, vol. 10, pp. 266-274, Mar 2011.

[3] Y. V. Pershin, and M. Di Ventra, "Practical approach to programmable analog circuits with memristors," IEEE Transactions on Circuits and Systems I-Regular Papers, vol. 57, pp. 1857-1864, Aug 2010.

[4] S. M. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H. –S. P. Wong, "An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation," IEEE Transactions on Electron Devices, vol. 58, pp. 2729-2737, Aug 2011.

[5] K. Seo, et al., "Analog memory and spike-timing-dependent plasticity characteristics of a nanoscale titanium oxide bilayer resistive switching device," Nanotechnology, vol. 22, p. 254023, Jun 2011.

[6] S. H. Jo, et al., "Nanoscale memristor device as synapse in neuromorphic systems," Nano Letters, vol. 10, pp. 1297-1301, Apr 2010.

[7] T. Chang, et al., "Synaptic behaviors and modeling of a metal oxide memristive device," Applied Physics A-Materials Science and Processing, vol. 102, pp. 857-863, Mar 2011.

[8] G. S. Snider, "Self-organized computation with unreliable, memristive nanodevices," Nanotechnology, vol. 18, p. 365202, Sep 2007.

[9] T. A. Wey, and W. D. Jemison, "Variable gain amplifier circuit using titanium dioxide memristors," IET Circuits Devices and Systems, vol. 5, pp. 59-65, Jan 2011.

[10] Y. V. Pershin, and M. Di Ventra, "Memory effects in complex materials and nanoscale systems," Advances in Physics, vol. 60, pp. 145-227, 2011.

[11] F. Alibart, L. Gao, B. Hoskins, and D. B. Strukov, "High-precision tuning of state for memristive devices by adaptable variation-tolerant algorithm," Nanotechnology, vol. 23, p. 075201, Feb 2012.

[12] K. K. Likharev, "Hybrid CMOS/nanoelectronic circuits: opportunities and challenges", Journal of Nanoelectronics and Optoelectronics, vol. 3, pp. 203-230, Dec 2008.

[13] C. H. Bishop, *Pattern Regcognition and Machine Learning*, *S*pringer, 2006.

[14] R. F. Coughlin, and F. F. Driscoll, *Operational Amplifiers and Linear Integrated Circuits*, 6th Edition, Prentice Hall, 2000.

[15] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, "Electrochemical metallization memories - fundamentals, applications, and prospects," Nanotechnology, vol. 22, p. 254003, Jul 2011.

[16] T. Hasegawa, K. Terabe, T. Tsuruoka, and M. Aono, "Atomic switch: atom/ion movement controlled devices for beyond von-neumann computers," Advanced Materials, vol. 24, pp. 252-267, Jan 2012.

[17] M. N. Kozicki, M. Park, and M. Mitkova, "Nanoscale memory elements based on solid-state electrolytes," IEEE Transactions on Nanotechnology, vol. 4, pp. 331-338, May 2005.

[18] K. Terabe, T. Hasegawa, T. Nakayama, and M. Aono, "Quantized conductance atomic switch," Nature, vol. 433, pp. 47-50, Jan 2005.


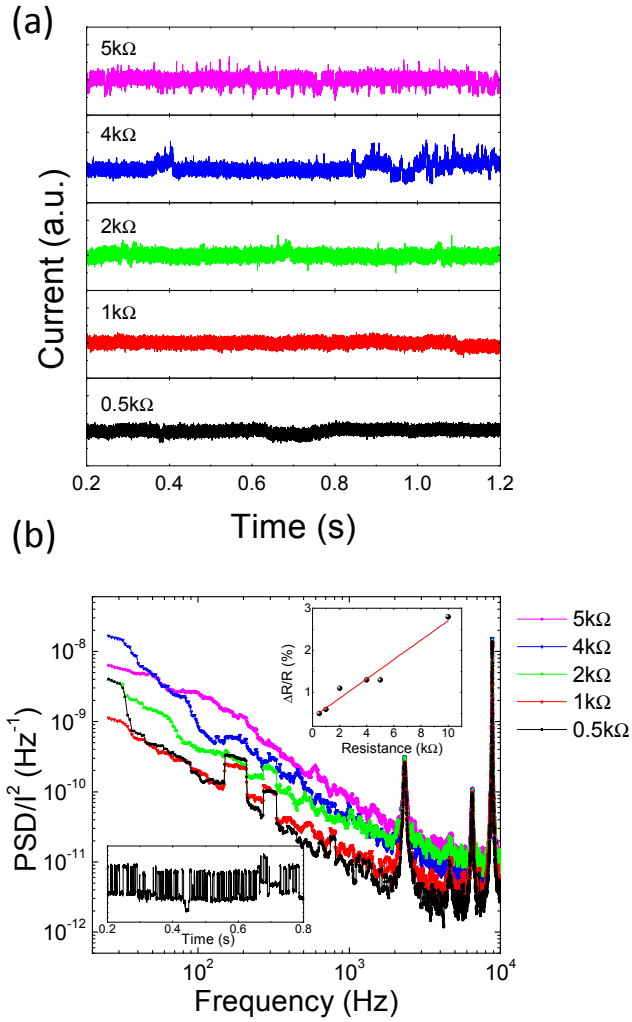


Figure 4. (a) The random telegraph noise signal for the device in different resistance states (0.5 kΩ, 1 kΩ, 2 kΩ, 4 kΩ and 5 kΩ, respectively) measured at 300 K under 0.1 V, and sampling rate of $10^4$ Sa/s. Noise amplitude is normalized by the value of the average current. (b) The spectral power density as a function of frequency for the corresponding resistance state. The bottom left inset shows a typical measurement of RTN noise at the highest resistance state (10 kΩ). The relative resistance fluctuations, $\Delta R/R$ against different resistance states, is shown in top right inset.


[19] U. Russo, D. Kamalanathan, D. Ielmini, A. L. Lacaita, and M. N. Kozicki, "Study of multilevel programming in programmable metallization cell (PMC) memory," IEEE Transactions on Electron Devices, vol. 56, pp. 1040-1047, May 2009.

[20] Y. C. Yang, F. Pan, Q. Liu, M. Liu, and F. Zeng, "Fully room-temperature-fabricated nonvolatile resistive memory for ultrafast and high-density memory application," Nano Letters, vol. 9, pp. 1636-1643, Apr 2009.

[21] H. X. Guo, et al., "The growth of metallic nanofilaments in resistive switching memory devices based on solid electrolytes," Applied Physics Letters, vol. 94, p. 153504, Apr 2009.

[22] R. Waser, and M. Aono, "Nanoionics-based resistive switching memories," Nature Materials, vol. 6, pp. 833-840, Nov 2007.

[23] S. H. Jo, K. H. Kim, and W. Lu, "High-density crossbar arrays based on a Si memristive system," Nano Letters, vol. 9, pp. 870-874, Feb 2009.

[24] S. H. Jo, K. H. Kim, and W. Lu "Programmable resistance switching in nanoscale two-terminal devices," Nano Letters, vol. 9, pp. 496-500, Jan 2009.

[25] S. H. Jo, and W. Lu, "CMOS compatible nanoscale nonvolatile resistance switching memory," Nano Letters, vol. 8, pp. 392-397, Feb 2008.

[26] K.-H. Kim, et al., "A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications," Nano Letters, vol. 12, pp. 389-395, Jan 2012.

[27] D. Lee, et al., "Noise-analysis-based model of filamentary switching ReRAM with $ZrO_x/HfO_x$ stacks," IEEE Electron Device Letters, vol. 32, pp. 964-966, Jul 2011.

[28] D. Ielmini, F. Nardi, and C. Cagli, "Resistance-dependent amplitude of random telegraph-signal noise in resistive switching memories," Applied Physics Letters, vol. 96, p. 053503, Feb 2010.

[29] R. Soni, et al., "Probing Cu doped $Ge_{0.3}Se_{0.7}$ based resistance switching memory devices with random telegraph noise," Journal of Applied Physics, vol. 107, p.024517, Jan 2010.

[30] M. Terai, Y. Sakotsubo, Y. Saito, S. Kotsuji, and H. Hada,"Memory-state dependence of random telegraph noise of $Ta_2O_5/TiO_2$ stack ReRAM," IEEE Electron Device Letters, vol. 31, pp. 1302-1304, Nov 2010.

[31] M. Terai, Y. Sakotsubo, Y. Saito, S. Kotsuji, and H. Hada, "Effect of bottom electrode of ReRAM with $Ta_2O_5/TiO_2$ stack on RTN and retention," in: Proc. Int. Electron Devices Meeting (IEDM), pp. 775-778, 2009.

[32] Y. H. Tseng, W. C. Shen, C. E. Huang, C. J. Lin, and Y. C. King, "Electron trapping effect on the switching behavior of contact RRAM devices through random telegraph noise analysis," in: Proc. Int. Electron Devices Meeting (IEDM), pp. 636-639, 2010.

[33] R. Sarpeshkar, "Analog versus digital: extrapolating from eletronics to neurobiology," Journal of Neural Computation, vol. 10, pp. 1601-1638, Oct 1998.