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Memristive devices for computing

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Table S1 Various insulator materials use in anion devices (VCM). Top electrode (TE), bottom electrode (BE), switching modes and references are also listed for each.

Insulators	Bottom Electrode	Top electrode	Switching mode	reference
MgO	Pt	Pt	Unipolar	1
TiOx	Ru, Pt	Al, Pt	Non/Uni/Bipolar	2, 3
ZrO_x	P^+-Si , n^+-Si	Pt, Cr	Uni/Bipolar	4-6
HfO_x	TiN	TiN	Bipolar	7
VO_x	N/A	N/A	Threshold	8, 9
NbO_x	P^+-Si	Pt	Unipolar	10
TaO_x	Pt, Ta	Pt, Ta	Bipolar	11, 12
CrO_x	TiN	Pt	Bipolar	13
MoO_x	Pt	Pt-Ir	Uni/Bipolar	14
WO_x	W, FTO	TiN, Au	Bipolar	15, 16
MnO_x	Pt	Al, TiN	Bipolar	17, 18
FeO_x	Pt	Pt	Non/Bipolar	19, 20
CoO_x	Pt	Pt	Nonpolar	21
NiO_x	Pt	Pt	Nonpolar/Threshold	22, 23
CuO_x	TiN, TaN, SRO, Pt	Pt	Bipolar	24
ZnO_x	Pt, Au	TiN, Ag	Bipolar	25-27
AlO_x	Ru, Pt	Pt, Ti	Unipolar/Bipolar	28, 29
GaO_x	ITO	Pt, Ti	Bipolar	30
SiO_x	Poly-Si, TiW	Poly-Si, TiW	Unipolar	31
SiO_xN_y	W	Cu	Bipolar	32
GeO_x	ITO, TaN	Pt, Ni	Bipolar	33, 34
SnO_2	Pt	Pt	Unipolar	35
BiO_x	Bi	W, Re, Ag, Cu	Bipolar	36
SbO_x	Pt	Sb	Unipolar/Bipolar	37
SmO_x	TiN	Pt	Bipolar	38
GdO_x	Pt	Pt	Unipolar	39
YO_x	Al	Al	Unipolar	40
CeO_x	Pt	Al	Bipolar	41
EuO_x	TaN	Ru	Uni/Bipolar	42, 43
PrO_x	TaN	Ru	Bipolar	42, 43
ErO_x	TaN	Ru	Unipolar	42, 43
DyO_x	TaN	Ru	Unipolar	42, 43
NdO_x	TaN	Ru	Unipolar	42, 43
$Ba_{0.7}Sr_{0.3}TiO_3$	$SrRuO_3$	Pt, W	Bipolar	44
$SrTiO_3$	$SrRuO_3$, Au, Pt	Au, Pt	Bipolar	45
$SrZrO_3$	$SrRuO_3$	Au	Bipolar	46
$BiFeO_3$	$LaNiO_3$	Pt	Bipolar	47
$Pr_{0.7}Ca_{0.3}MnO_3$	YBCO, Pt, $LaAlO_3$	Ag	Bipolar	48
$La_{0.33}Sr_{0.67}FeO_3$	Au	Al	Bipolar	49
$Pr_yLa_{0.625-y}Ca_{0.375}MnO_3$	Ag	Ag	Bipolar	50
Nitrides (AlN)	Al, TiN, Pt	Al, TiN, Pt	Bipolar	51
Telluride (ZnTe)	Si	Au	Bipolar	52
selenide (ZnSe)	P^+-Ge	In, In-Zn	Bipolar	53
Polymers	Al, ITO, Cu	Al, ITO, Cu	Bipolar	54, 55

Table S2 | Various electrolyte materials used in cation devices (electrochemical metallization memory). Top electrode, bottom electrode, switching modes and references are also listed for each.

Electrolytes	Bottom Electrode	Top electrode	Switching mode	reference
Sulfides:				
Ge_xS_x	W	Ag	Bipolar	56
As_2S_3	Au	Ag	Bipolar	57
Cu_2S	Cu	Pt	Bipolar	58, 59
$Zn_xCd_{1-x}S$	Pt	Ag	Bipolar	60
Iodides:				
AgI	Pt	Ag	Bipolar	61
$RbAg_4I_5$	Pt	Ag	Bipolar	62
Selenides:				
Ge_xSe_y	W	Ag, Cu	Bipolar	63
Tellurides:				
Ge_xTe_y	TiW	Ag	Bipolar	64
Ternary chalcogenides:				
Ge-Sb-Te	Mo	Au, Ag	Bipolar	65
oxides				
Ta_2O_5	Pt	Cu	Bipolar	66
SiO_2	W	Cu	Uni/Bipolar	67
HfO_2	Pt	Cu	Bipolar	68
WO_3	Pt	Cu	Bipolar	69
ZrO_2	Ag	Au	Bipolar	70
$SrTiO_3$	Pt	Ag	Bipolar	71
TiO_2	Pt	Ag	Bipolar	72
CuO_x	Cu	Al	Unipolar	73
ZnO	Pt, Al doped ZnO	Cu	Bipolar	74
Al_2O_3	Al	Cu	Bipolar	75
MoOx	Cu	Pt	Bipolar	76
GdO_x	Pt	Cu doped MoO_x		77
Others:				
MSQ	Pt	Ag	Bipolar	78
doped organic semiconductors	Pt	Cu	Bipolar	79
nitrides	Pt	Cu	Bipolar	80
amorphous Si	P^+-Si	Ag	Bipolar	81
Carbon	Pt	Cu	Bipolar	82
vacuum gaps	$RbAg_4I_5$/Ag, Ag_2S/Ag	W, Pt	Bipolar	83, 84

Table S3 | Quantitative estimates for required performance metrics. Color indicates fidelity of the estimates, with black color standing for high fidelity, e.g. due to reported values in ITRS [85], blue color for moderate fidelity, e.g. representative of some limited simulations which cannot be generalized for all cases, and red color for poorly understood requirements, obtained by general considerations but not supported with rigorous simulations.

	Storage(*)	Memory(*)	Logic	Neuro	Best reported	Comments
Reproducibility	< 10% [86] (1a)	< 1% [86] (1a)	< 20 % [87] (1b)	< 50% [88, 89] (1c)	few percent (1d) [90]	The numbers are for so called "stuck-on-open" defects while the requirement for other type of defects might be stricter. (1a) More efficient error correcting codes requiring large decoding latency are used in storage application. (1b) A smaller number of defects could be required for high fan-in digital logic. (1c) These applications are also quite tolerant to variations in the switching behavior [91, 92]. (1d) The number has still to be confirmed for crossbar circuits operation (only one memristor is turned to the ON state at a time in Ref. [90] while others are always kept in the OFF state).
Endurance	> 10^4 (#)	> 10^{16} (#)	>100 (&, 2a)	>100 – 10^6 (2b)	10^{12} [93]	(2a) The endurance requirement for material implication logic [94] is much higher, similar to that of memory. (2b) Larger number is for in-situ –trained networks which require modification of the weight upon learning and more demanding as compared to simple weight import with ex-situ training.
Switching energy	< 1 pJ (3a)	< 5 fJ (#)	not critical (&)	not critical (&)	1 pJ [95, 96]	(3a) Should be within allowable power budget (but still large enough to cause local heating)
Switching speed	< 10 µs (#)	< 1 ns (#)	not critical (&, 4a)	not critical (&, 4a, 4b)	100 ps [97]	(4a) Given an appropriate amount of parallelism, very slow writes might be okay. (4b) For in-situ training the speed should be fast enough to provide reasonable training time, e.g. to implement <10^6 training epochs
Retention	>10 years (#)	> minutes - month (5a)	> days (&, 5b)	> seconds - days (&, 5c)	10^{14} [98]	(5a) Volatile memory might be still okay for many memory applications [99]. (5b) Infrequent refresh might be okay provided that it is much shorter than the operating time. (5c) For spiking networks a broad range of relaxation times (volatility) might be required [100].
ON/OFF current ratio	> 10 (6a)	> 50 (6a)	> 100	> 500 (6b)	> 10^{11} [6, 101-103]	(6a) ON/OFF current ratio affects the speed and power consumption. (6b) The requirement might be relaxed by increasing the number of states.
OFF state Resistance	> 1 MΩ	> 100 kΩ	> 10 MΩ	>100 MΩ	1kΩ – 100 GΩ [101]	In general, the requirement for OFF resistance (at operating voltage) is determined by the static leakage power consumption, which is the largest in case of logic and neuromorphic applications due to their massively parallel operation. The requirement is also indirectly affected by the desired ON resistance for a given ON/OFF ratio. The ON resistance should be large enough that the voltage drop across the crossbar wire is negligible (to ensure write operation) and that the sizing (overhead) of the CMOS drivers is minimal.

I-V nonlinearity	> 100-10000 [(8a)]	> 100-1000 [(8a)]	> 10 [(8b)]	not critical [(8c)]	100 [104]	Nonlinearity is defined as $I(V_{WRITE})/I(V_{WRITE}/2)$ or $I(V_{WRITE})/I(-V_{WRITE})$ and the requirement in general scales with the number of half-selected devices (i.e. *N*). (8a) The requirement strongly depend on the read-out scheme and other device parameters which determine acceptable *N* [New Ref. 1] (8b) The smallest because crossbar might be depopulated without much performance degradation. (8c) Purely linear synapses are acceptable for correct operation. Whether nonlinearity would enhance circuit performance is not well understood.
Number of states	2-16 [(9a)]	2 [(9a)]	2-16 [(9b)]	2-32 [(9c)]	~ 100 [105]	(9a) In general, the more states, the better the density is, however, at the expense of write and read latency. (9b) A larger number of states allows for more complex circuits, e.g. based on linear threshold logic [106]. (9c) The performance (e.g. for classification task) approaches its maximum value with ~5-bit weights.
density	> $(10\ nm)^{-2}$ and > 4 layers [(#)]	> $(10\ nm)^{-2}$ [(#)]	> $(20\ nm)^{-2}$ & multilayer [(10a, 10b)]	> $(10 - 100\ nm)^{-2}$ & multilayer [(10a, 10c)]	4 layer [107] $1/(10\ nm)^2$ [108]	(10a) Density is constrained by CMOS circuits. (10b) Only a small fraction of memristive devices are actively employed, i.e. turned to the ON state, for typical applications so that depopulated crossbars with relatively large devices could be acceptable without losing much routability. (10c) The higher density number would allow to exceed the density of bio-cortical circuits [109].

Common footnotes: (#) The performance should be comparable or better than projected values by ITRS in order to compete with other emerging technologies, i.e. NAND flash and SRAM for storage and memory applications, respectively [85]. (&) The requirement is relaxed due to relatively infrequent changes to memristive state in these applications. (*) Because area overhead associated with peripheral circuitry increases linearly with linear crossbar size *N*, while the useful area scales as N^2, naturally the larger arrays are more area efficient, however, at the expense of latency (because of larger *RC* delay) and possibly write/read energy [86]. The density (i.e. cost) should be more important for storage applications demanding larger array sizes as compared to that of fast memory applications.

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