Digital-to-Analog and Analog-to-Digital Conversion with Metal Oxide Memristors for Ultra-Low Power Computing

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Abstract— The paper presents experimental demonstration of 6-bit digital-to-analog (DAC) and 4-bit analog-to-digital conversion (ADC) operations implemented with a hybrid circuit consisting of Pt/TiO$_2$/Pt resistive switching devices (also known as ReRAMs or memristors) and a Si operational amplifier (op-amp). In particular, a binary-weighted implementation is demonstrated for DAC, while ADC is implemented with a Hopfield neural network circuit.

Keywords— ReRAM; memristor; Digital-to-analog conversion; Analog-to-digital conversion; Hopfield neural network; hybrid circuits

I. INTRODUCTION

Analog computing presents an attractive alternative for data processing that demands extraordinary energy efficiency. However, as pure analog circuits cannot address the noise accumulation problem, a practical solution would require inclusion of analog-to-digital and digital-to-analog stages for signal restoration [1]. Highly energy-efficient data converters are therefore expected to play an important role in future computing platforms and thus new ways of implementing compact and ultra-low-energy data converters are therefore of significant relevance.

One promising technology particularly suited for analog computing is the hybrid circuits which integrate CMOS and memristor devices [2-5]. Memristors are essentially two-terminal thin-film devices whose resistances can be tuned in a nonvolatile and analog way [6-15]. In the context of analog circuit applications, recent advances in memristive devices and their integration with CMOS enable efficient implementations of nanoscale analog-grade resistive elements which can be fine-tuned after fabrication [16]. In this paper, we demonstrate binary-weighted DAC and Hopfield-network ADC circuits which utilize the feature of post-fabrication resistance tuning for achieving energy-efficient conversion.

II. MEMRISTIVE DEVICES

Fig. 1 shows typical $I$-$V$ characteristics of TiO$_{2-x}$ memristive devices, which are obtained by a quasi-DC
triangular voltage sweep from 0 to 1.5V followed by a quasi-DC triangular current sweep from 0 to -1mA. The device structure and fabrication methods are similar to the ones described in Ref. [16]. Additionally, nanoscale metallic protrusion has been implemented in each device in order to localize the switching region (Fig. 2a). This technique, while not required for truly nanoscale devices, helps improve the yield (from about 60% for the blanket film devices to 95%+ for devices with protrusion, as shown in Fig. 2b) and significantly lower the variations in their switching behaviors.

III. BINARY-WEIGHTED DAC

Fig. 3 shows a schematic diagram of a 6-bit DAC following a binary-weighted style. The circuit consists of 6 memristors and an op-amp with a negative feedback resistor $R_f$. For a set of digital input voltages $V_i$ (where $i$ is from 0 to 5) the analog output voltage $V_{out}$ can be expressed as $-R_f/2 \times \sum_2^5 V_i$, when the $i^{th}$ memristor is tuned to a state with a conductance of $2^i/R$. The circuit is implemented with a discrete integrated circuit (IC) op-amp (ST TL074) and a packaged memristor chip wired manually on a breadboard.

During the programming stage, memristors are set to the desired states with high precision (~1% error) with the help of automated feedback-based algorithm [16] using relatively large programming voltages $|V| > 0.5$V whereas input voltage is always limited to 0.2V during operation which has been shown to cause negligible drift to the state in the considered memristors [16]. The experimental results for a 6-bit DAC are shown in Fig. 4, and its differential nonlinearity (< 0.11 LSB) and integral nonlinearity (< 0.17 LSB) characteristics are shown in Figs. 5a and b, respectively. Because of the quasi-DC testing condition, the main contributing factor to the nonlinearity is proven to be random telegraph noise [6, 17-20] in the high resistance states (Fig. 6).

![Figure 3](image3.png)

Figure 3. A schematic of 6-bit binary-weighted digital-to-analog converter implemented with hybrid circuits. Memristors are programmed to have conductances (at 0.2V) 40μS, 80μS, 160μS, 320μS, 640μS, and 1280μS. The circuit utilizes op-amp (with the feedback resistor $R_f$ = 3.3kΩ) to form the weighted sum of all input pulses applied to memristors.

![Figure 4](image4.png)

Figure 4. Measured transfer characteristics of a 6-bit DAC as a function of input code. The voltage step (≈ 26mV) can be seen clearly in the inset of the figure.

![Figure 5](image5.png)

Figure 5. (a) The differential nonlinearity (DNL) and (b) integral nonlinearity (INL) measured in least significant bits (LSB) as a function of input code for a 6-bit DAC.

IV. HOPFIELD NETWORK ADC

A 4-bit ADC implemented with a Hopfield neural network is shown schematically in Fig. 7a [21]. It consists of four inverting amplifiers (neurons), each of which is made with three IC op-amps (Fig. 7b), and a 4×6 memristor crossbar which defines the connectivity among neurons (and bias). The weights of recurrent part of the network, represented by the conductances of memristors which are listed in Fig. 8, are symmetrical with zero entries in the principal diagonal and $T_{ij} = 2^{(i-j)}$ otherwise, whereas the weights which are serving bias the voltage $V_R$ are $T_{IR} = 2^{(i-1)}$. The analog input $V_S$ is supplied
via fixed IC resistors of weight $2^i$ [21]. In other words, each neuron gets its input as a weighted sum of three different set of signals: reference bias $V_R$, the analog input voltage $V_S$, and four ADC circuit outputs, i.e. $V_1$ through $V_4$. Fig. 9a shows the measured output voltage for a quasi-DC sweep of input $V_S$ from 0 to 3.7V, while Fig. 9b shows the corresponding binary output code. In order to achieve a properly functional circuit, all neurons are reset periodically to ‘zero’, which helps avoid getting stuck in local minima. Additionally, non-ideal behaviors of neurons (most importantly the offset voltage in op-amps) are compensated by fine-tuning bias weights.

V. SUMMARY

We have experimentally demonstrated hybrid circuit implementation of DAC and ADC. The demonstrated work is a proof of concept for using memristors as high-precision weights in conversion circuits. At least for relatively low-precision (< 8 bit) data processing the considered approach could be very compact and energy efficient due to high density of analog weights implemented with memristive devices.

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REFERENCES

The conductance values of the memristors used in the ADC circuit. Resistors $R_1$, $R_2$, and $R_3$ are used in the neuron circuit to ensure either a 0 or -0.2V output.

![Table](image)

**Figure 8**

**Figure 9** (a) Measured output voltage of the ADC circuit and (b) the corresponding digital code as a result of an application of analog input voltage ramp (shown with red in panel b) which is varied from 0 to its maximum value. The outputs of the neurons are periodically reset with a frequency of 80Hz.


