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Utilizing NDR effect to reduce switching threshold variations in memristive devices

Fabien Alibart · Dmitri B. Strukov

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Abstract Variations in the switching threshold voltage of memristive devices present significant challenges for their integration into large-scale circuits. In this paper, we propose to address this problem by adding a device exhibiting S-type (N-type) negative differential resistance (NDR) in series (parallel) with memristive devices. The main effect comes from the transition between low- and high-conductivity branches of the NDR device, which leads to a redistribution of the voltage drop inside the device stack, and, as a result, the effective lowering of variations in the switching threshold. The idea is checked experimentally using a TiO_{2-x} memristive device connected in parallel with a tunnel GaAs diode.

1 Introduction

Thin film devices exhibiting resistive switching ("memristive" [1]) effect [2–5] have a potential to significantly improve performance for a variety of applications, including digital memories, reconfigurable digital and analog, and neuromorphic computing circuits—see, e.g., recent reviews in Refs. [6–10]. While some of the applications, such as artificial neural networks, are to some extent defect- and variation-tolerant [6, 11], the performance of others is greatly impacted by variations in I–V characteristics of the memristive devices.

In the context of passive crossbar circuits [6, 9, 10], variations in the switching threshold are particularly troublesome. For example, Fig. 1 shows superimposed "SET" transitions of eight switching cycles for six TiO_{2-x} devices. All the devices are implemented with an e-beam defined protrusion (inset of Fig. 1a) to improve yield and reduce variations in switching behavior. While this technique has led to much better devices (as compared to those without artificial filament [12]), there are still significant variations across different devices and even dispersion in I–V characteristics for different switching cycles for the same device. (Such variations are somewhat representative and similar to the other reported data [5, 6].)

In principle, a much larger voltage (as compared to the threshold one) could be applied in order to force a SET transition with high fidelity in the presence of such variations. For example, for the statistics in Fig. 1, the write voltage $V_w \gtrsim 2.2$ V would be needed to ensure that the selected device will be set at all times. On the other hand, half of the write voltage is applied to half-selected devices in dense passive crossbar structures [6]—e.g. devices 2 and 3 in the Fig. 1b inset. For the switching threshold statistics, the half bias $V_w/2 \approx 1.1$ V should not disturb the devices with the smallest switching threshold (which is about 1.25 V from Fig. 1). However, the tails in the switching threshold distribution will be certainly broader when larger statistics are considered. That means that, in a more realistic scenario, larger voltages should be applied to ensure SET switching and that there will always be half-selected devices which would be set inadvertently.

For example, assuming that the voltage threshold is normally distributed with $\mu = 1.66$ and $\sigma = 0.28$, voltage $V_{SET^*} \approx \mu + \sqrt{2}\sigma\,\mathrm{erfc}^{-1}(1 - 2/N) \approx 2.46$ V is needed to ensure only one failure on average in $N = 10^3$ writes, which would be equivalent to one error per second on average when writing the device every 1 ms. This means that above $0.5 + 0.5\,\mathrm{erf}[(\frac{V_{SET^*}}{2} - \mu)/\sqrt{2}\sigma] \approx 0.095$ fraction of half-selected devices will be disturbed in each write opera-

F. Alibart · D.B. Strukov (✉)
Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA 93106, USA
e-mail: strukov@ece.ucsb.edu

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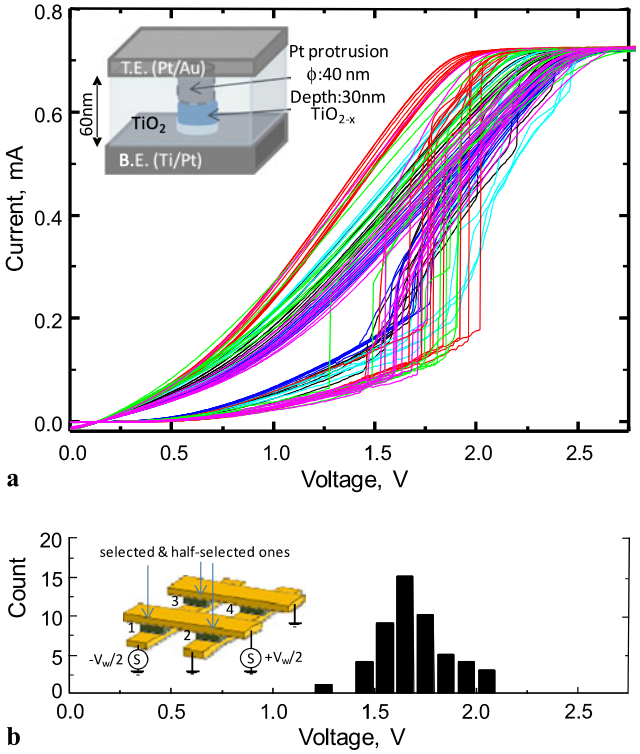

Fig. 1 (**a**) Typical SET switching of TiO_{2-x} devices: (*bottom*) 48 superimposed I–Vs showing SET transitions and (**b**) histogram for apparent switching threshold voltage. In particular, six devices have been tested and each color represents 8 SET switching transitions for the same device. The *insets* in the *top* and *bottom panels* show schematic representations of the device and a 2×2 passive crossbar circuit explaining the half-select problem, correspondingly. Saturation at ~0.7 mA is due to current compliance

tion, which might be unacceptable for the proper memory operation.

The situation is further exacerbated by the fact that the rate of switching is typically (super) exponentially dependent on applied voltage [13], which is certainly true for the devices considered in this paper [12], so that the notion of a voltage threshold is just a convenient simplification. The effect of gradual change of the memristive state is neglected in the example above, and so in reality the fraction of disturbed devices would be even larger.

2 Main idea and experimental results

Figure 2 explains the proposed technique for lowering threshold variations. Suppose that a voltage bias ramp is applied across the device stack consisting of S-type NDR and memristive devices connected in series (Fig. 2a). Assuming particular I–V characteristics of the NDR and memristive devices chosen for the demonstration in Fig. 2a, at first the voltage is mostly dropped across the NDR layer. Upon increasing the external voltage (to about 1 V), the voltage

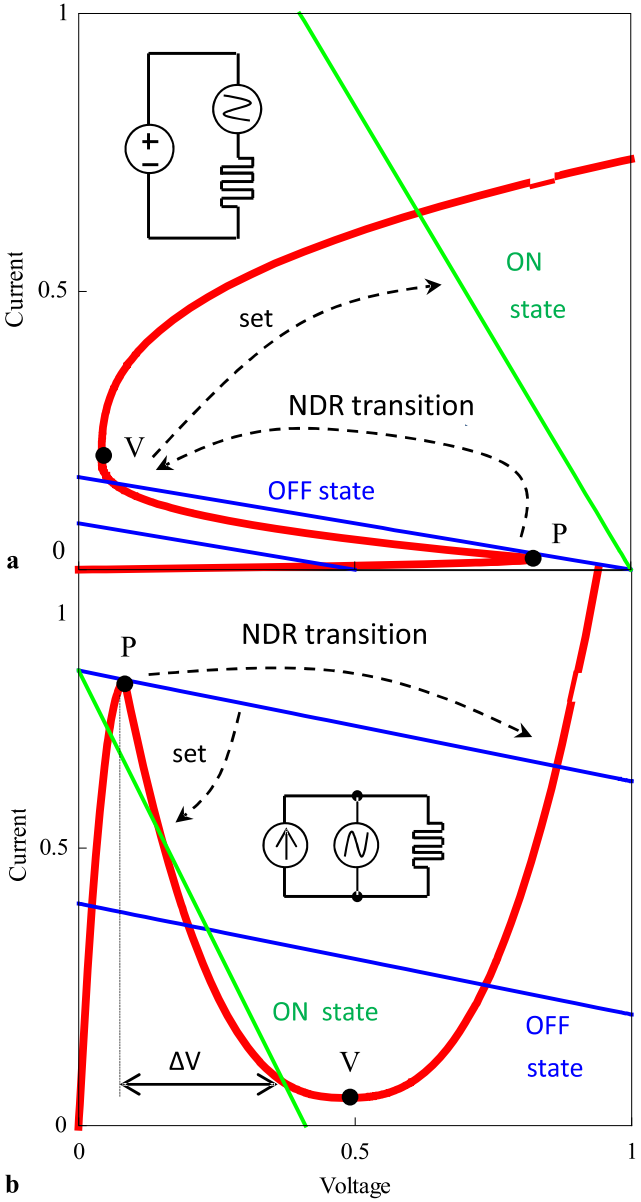

Fig. 2 Illustration of the threshold voltage variation reduction technique for (**a**) S-type and (**b**) N-type NDR devices, respectively. In *both panels red lines* show $I_{NDR}(V_{NDR})$ of the NDR devices, where V_{NDR} and I_{NDR} are voltage drop and current via the NDR device, respectively, shown in arbitrary units. A pair of *blue* (one *green*) *lines* show $I(V - V_{NDR})$ on (**a**) and $V(I - I_{NDR})$ on (**b**) for OFF (ON) states of memristive devices, correspondingly. A pair of blue lines corresponds to two values of applied voltage (**a**) or current (**b**) before and during the transition between different current branches in the NDR device. Points P, V denote peak and valley positions on the I–Vs of the NDR devices

drop across the NDR device reaches peak value (point P at Fig. 2a). At this moment, a transition from a high- to low-resistive branch of the NDR device occurs, which leads to an increase (from about 0.15 V to 0.95 V in Fig. 2a) in voltage across the memristive device. This transition is followed immediately by switching to the ON state (i.e. the

SET transition) if the new voltage across the memristive device is larger than the threshold one. Therefore, the overall effect due to such internal redistribution of the voltage between the NDR and memristive devices is a sharp increase in voltage from some low value (ideally zero voltage) to some large value (ideally the external voltage) across the memristive device. In the context of the half-select problem, the resulting step-like external—internal voltage transfer characteristics helps to ensure negligible internal voltage across the half-selected memristive devices when sufficiently large voltage is applied to switch the selected device.

There are plenty of physical mechanisms to achieve an S-type NDR, e.g. due to Joule heating [14], interband tunneling [15, 16], and instabilities in electronic conductions [17, 18]—see e.g. the comprehensive review in Refs. [19, 20]. Moreover, S-type NDR features could be intrinsic to the memristive devices in some cases [21, 22]. However, because S-type discrete integrated circuit components are not readily available, we have experimentally checked the proposed concept using GaAs Esaki diodes [23], which feature N-type NDR characteristics. In this case, to have a similar effect of voltage redistribution, N-type NDR and memristive devices are connected in parallel and driven by a current source (Fig. 2b). For demonstration, we used in-house fabricated TiO_{2-x} memristive devices. The fabrication conditions for memristive devices are similar to previously reported results [12], except that we used a nanoscale protrusion technique to improve yield and lower variations in the memristive devices. In particular, before deposition of the top electrode, a nanohole, which is 30 nm deep and about 50 nm in diameter, was locally defined by e-beam lithography on top of the TiO_2 film. The photoresist was used as a mask for dry etching of the nanohole into the TiO_2 layer. The top electrode was then deposited by e-beam evaporation.

Figure 3a shows the SET switching transitions when the device stack (i.e. the N-type NDR device in parallel with the memristive device shown in Fig. 2b) is driven by the current-controlled source. Upon application of the current ramp, there is a transition between low- and high-current branches of the GaAs device, which leads to a momentary increase in the external (measured) voltage by about 1 volt across the stack, and switching to the ON state of the memristive devices for most of the cases. Since the change in external voltage is only present in a current-controlled switching setup, Fig. 3a is redrawn by removing the voltage increase (shown schematically as ΔV in Fig. 2b) in Fig. 3b to highlight the effect of tightening of variations. A very crude estimate shows that for the same $V_{SET^*} = 2.46$ V the fraction of the disturbed devices is greatly reduced, potentially to below $<10^{-10}$, again assuming normally distributed statistics for the SET switching threshold.

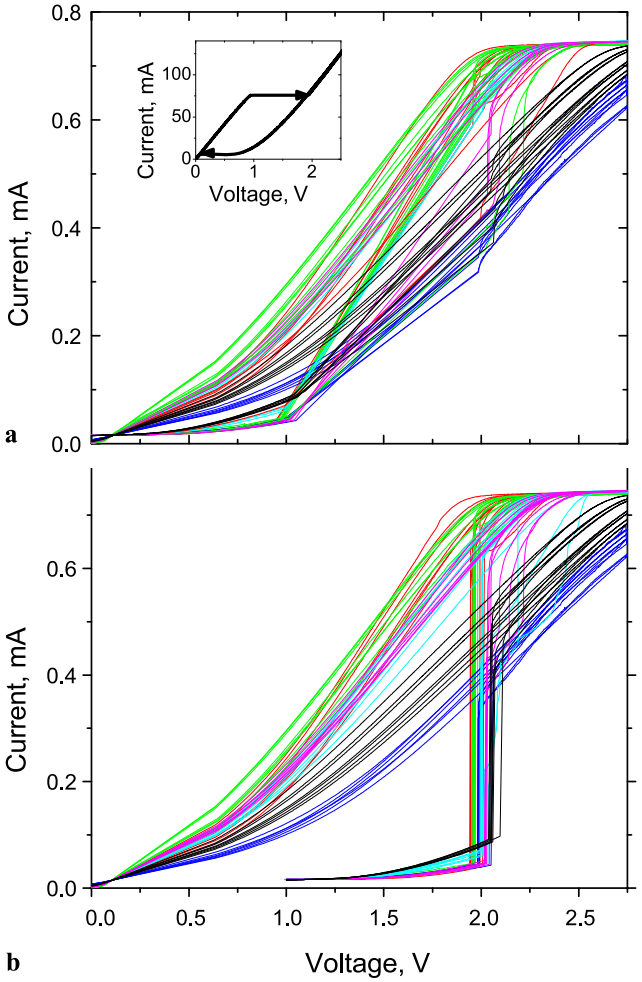

Fig. 3 Current-controlled SET switching I–Vs for memristive devices connected in parallel with GaAs N-type NDR devices (Esaki diode): (**a**) measured I–V curves via the memristive device and (**b**) the same I–V curves but with the removed voltage increase shown on panel (**a**). The *inset* of (**a**) shows measured current through the GaAs NDR device as a result of the voltage sweep

3 Discussion and summary

The SET process is typically variation-prone, in part due to very strongly nonlinear switching dynamics, and that is why in this paper we focused on lowering variations for the SET transition. In case RESET variations are not negligible, one solution would be to perform a write operation by first resetting all devices in the crossbar and then setting specific ones—just like in NAND flash memories. Since the RESET operation has to be performed for all devices, in this case the half-select problem will not be an issue, and one can simply use a large enough voltage to enforce RESET.

Another simplification is that the demonstration in our paper involves an N-type discrete device. In order for this technique to be practical, an S-type NDR element with dimensions matching the memristive device and specific parameters must be utilized. Most importantly, such an S-type

device should offer high-current density and provide suitable voltage/current peak and valley values. Also, for bipolar devices such an S-type NDR device should have high conductance for the negative voltages so that it does not interfere with the RESET transition. In addition, NDR devices should have significantly lower variations as compared to those of memristive devices. Whether such an S-type device can be engineered remains to be seen, though the variety of plausible mechanisms reported in the literature [19, 20] seems to be very encouraging.

It is also worth noting that, in principle, adding a nonlinear element in series [24, 25] would increase voltage threshold and, therefore, relax the problem of disturbing half-selected devices; however, it will also require applying large voltages and hence will increase dynamic power consumption for read and write operations. On the contrary, at least for the demonstrated case there is no increase in the operating voltage. Also, note that the suggested idea is different from the one in which the NDR device is used to provide select functionality [26–29], even though the device stack is essentially the same (i.e. an S-type NDR device in series with a memristive device). The main idea of using NDR as a select element is to decrease the leakage currents by increasing nonlinearity in the crosspoint device I–V.

To summarize, in this paper we propose a novel approach to addressing switching threshold variation problems by integrating an additional element exhibiting negative differential resistance characteristics (NDR) in the device stack. Such an approach allows for significant reduction in the dispersion of the switching threshold for the combined device stack and, in general, can be used synergistically with more conventional techniques for coping with variations, such as localizing the active switching area by defining an artificial protrusion and/or reducing the size of the electrodes.

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