

# Endurance-write-speed tradeoffs in nonvolatile memories

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**Abstract** We derive phenomenological model for endurance-write time switching tradeoff for nonvolatile memories with thermally activated switching mechanisms. The model predicts linear to cubic dependence of endurance on write time for metal oxide memristors and flash memories, which is partially supported by experimental data for the breakdown of metal oxide thin films.

## 1 Introduction

Nonvolatile memory devices require very strong nonlinearity in switching kinetics with respect to applied write stimulus (e.g., applied voltage), which is necessary to combine long retention with fast intrinsic write speed [17]. For example, the retention-to-write-speed ratio is more than 10 orders of magnitude for nonvolatile NOR/NAND flash memories (e.g., with 10 years of retention and microsecond/millisecond write time), while it is <6 orders of magnitude (tens of milliseconds retention and tens of nanoseconds write time) for volatile dynamic random access memories (DRAM) [6]. Given typical strong nonlinearity in switching mechanism, a very natural way to enhance this ratio in nonvolatile memories is to increase write speed by applying larger stress; however, larger stress is more harmful for device endurance, because the kinetics of the failure mechanisms is also typically strongly enhanced by larger write stress.

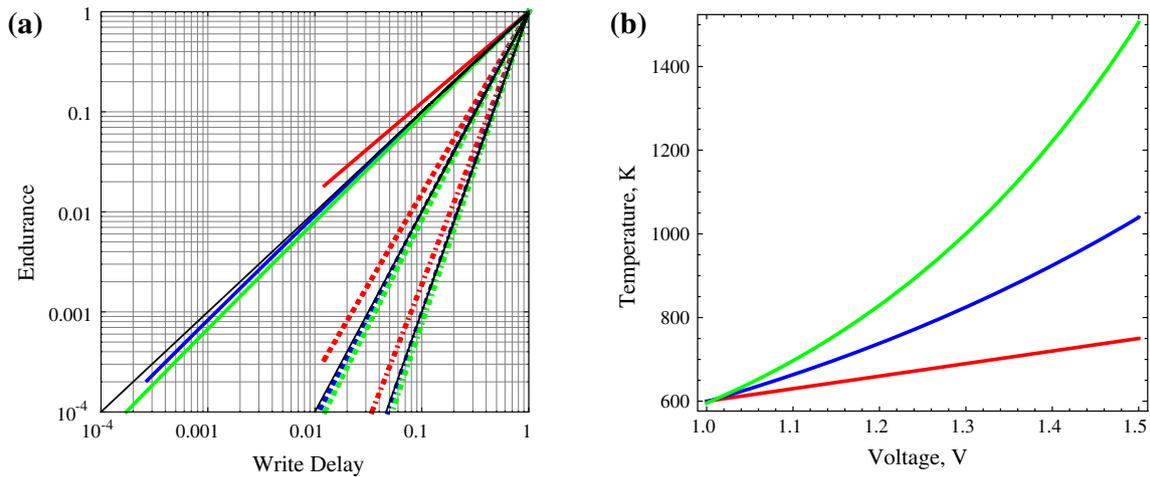
For example, in flash devices, the nonlinearity is due to (super-) exponential dependence of tunneling current on the applied electric field across gate/floating gate oxides. To get high retention-to-write-speed ratio, the electric fields might be close to 10 MV/cm [9], which is already very close to typical dielectric breakdown values in SiO<sub>2</sub> [11]. Increasing write (program/erase) voltages, in principle, will super-exponentially decrease write time [9]; however, it will also increase exponentially probability of creation of and/or filling of existing deep traps [11], which are the primary reason for limited endurance in flash memories.

A similar endurance-write-speed tradeoff exists for the emerging nonvolatile memories. In valence-change, electrochemical, and thermochemical memories [18] (which are often called ReRAM [6] or memristors [5]), the write speed is very often super-exponential function of applied voltage [17]—see for example, experimental evidence of that for valence-change memories in Refs. [1, 13]. The primary memory mechanism is due to ion profile modulation, such as motion of oxygen vacancies in valence-change and thermochemical memories, or motion of electrode material ions in electrochemical memories. The ionic motion in solids is thermally activated process with exponential dependence on the electric field [12], and, therefore, whenever Joule heating is involved, the switching kinetics is strongly super-exponential [17]. Though there are limited studies of the failure mechanisms in memristive devices, at least preliminary evidence shows that one of the mechanisms is related to the overstressing devices upon write operation. Very high temperatures combined with high electric field can cause melting of the electrode material (or a formed filament) inside the insulating matrix causing permanent failure. Given the thermally activated nature of the failure mechanisms, it is natural to expect that endurance would decrease (super-) exponentially with applied stress.

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**Fig. 1** **a** Normalized endurance versus normalized write delay for three values of  $U_F = 2$  eV (solid lines), 3 eV (dashed), and 4 eV (dot-dashed) and **b** three functions of  $T = f(V)$ —i.e., linear (red), exponential (blue), and steep exponential (green). Other assumptions are that  $U_S = 1$  eV,  $a/d = 0.1$  and that applied voltage  $V$  is changing

Endurance failure mechanisms have been studied extensively in the past for flash memories [3] and recently in metal oxide resistive switching devices [4, 8]. However, to the best of our knowledge, the endurance-write-speed tradeoffs were never studied analytically and the main goal of this paper is to derive such model. Our particular goal is to study catastrophic failures, such as electrode stability or oxide degradation [4], as opposed to the endurance problems which can be recovered from by reconditioning the device (e.g., resulted from repetitively applying asymmetric set/reset stress when switching the device on and off).

## 2 Phenomenological model

To derive endurance-write-speed tradeoff, let us assume a model loosely based on the one presented in Ref. [15]. In particular, let us assume that in case of memristors (flash memories) to switch memory state of the device an ion (electron) must travel the distance  $d$  across insulating matrix (gate oxide) upon application of write voltage  $V$ . Assuming thermally activated motion with activation energy  $U_S$  and local thermal temperature  $T$ , and constant electric field, the switching speed can be approximated as

$$t_S \approx \frac{d}{v_S} \approx \frac{2d}{fa} \exp\left[\frac{U_S}{kT}\right] \exp\left[-\frac{Vq a}{2kT d}\right], \quad (1)$$

where  $v_S$  is a speed of ions (electrons),  $k$  is a Boltzmann constant,  $q$  is an elementary charge,  $f$  is the frequency of escape attempts, and  $a$  is an average hopping distance [15]. The temperature is also a function of voltage when Joule heating is involved, i.e.,

from 1 to 1.5 V. Both write delay and endurance for every particular tradeoff curve are normalized with respect to the slowest write time and the highest endurance. Solid black lines are just guides for an eye showing linear, quadratic, and cubic endurance–write delay relations

$$T \approx 300 \text{ K} + IV \quad (2)$$

Let us assume that the failure mechanism is due to thermally activated motion of ions (electrons) across the distance  $d$  but with higher activation energy  $U_F$ , so that average time to failure is

$$t_F \approx \frac{d}{v_F} \approx \frac{2d}{fa} \exp\left[\frac{U_F}{kT}\right] \exp\left[-\frac{Vq a}{2kT d}\right]. \quad (3)$$

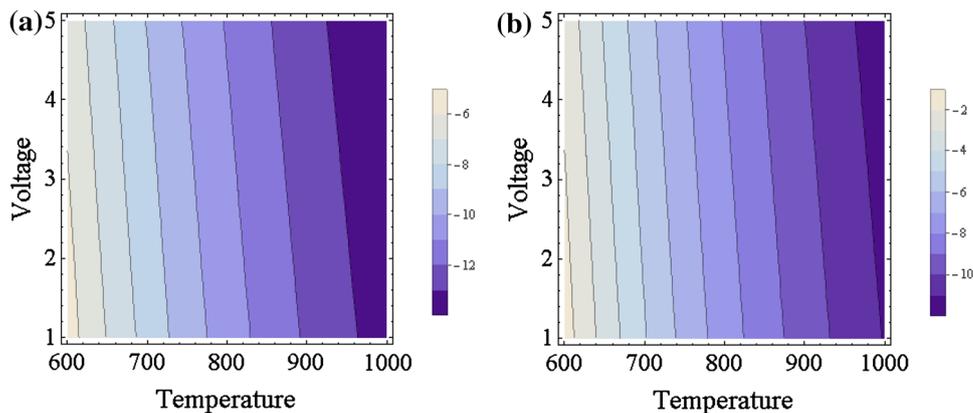
With such definition, the endurance, i.e., the number of times the devices can be switched before the failure occurs, is proportional to the ratio of failure to switch times:

$$\text{Endurance} \approx t_F/t_S. \quad (4)$$

Figure 1a shows endurance-write-speed tradeoff data calculated with Eqs. 1–4 for several plausible temperature–voltage dependences (Fig. 1b). The considered temperature dependences are phenomenological and based on typically observed local temperatures and possible heating mechanisms. For example, a quadratic dependence is representative of ohmic conductance, while exponential dependence is representative of exponential tunneling current transport [2]. For all cases, it is assumed that the local temperature is 300 K at 0 V and 600 K for 1 V applied voltage.

In particular, Fig. 1a shows that if the activation energy for failure mechanism is not too high and only by 1 eV larger than that of switching, which would be representative of low-endurance devices, the increase in speed is linearly proportional to the decrease in endurance. For larger  $U_F$ , the increase in speed results in approximately quadratic and cubic drop in endurance for  $U_F = 3$  and

**Fig. 2** Estimated write delay (shown in seconds on a log scale) as a function of internal temperature (in Kelvin degrees) and applied voltage (in V) for **a**  $U_S = 1.0$  eV and **b**  $U_S = 1.2$  eV and  $d = 10$  nm,  $a = 0.2$  nm, and  $f = 10^{13}$  Hz



4 eV, correspondingly. The results show that the tradeoff is mostly determined to the difference between  $U_F$  and  $U_S$  and almost insensitive to the particular law of temperature dependence and other parameters. Moreover, for relatively small electric field  $Vqa \ll 2dU_S$  the following approximate formula can be used:

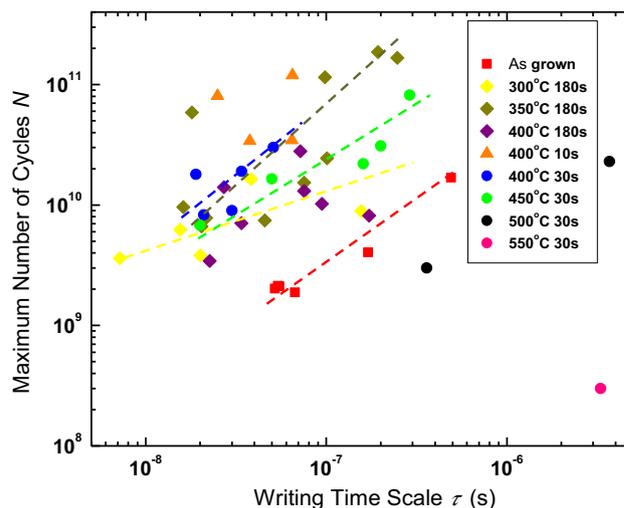
$$\text{Endurance} \approx \left(\frac{t_S}{t_0}\right)^{\frac{U_F}{U_S}-1}, \tag{5}$$

where  $t_0 = 2d/(fa)$ .

### 3 Discussion and summary

Assuming reasonable values of  $d = 10$  nm,  $a = 0.2$  nm, and  $f = 10^{13}$  Hz results in  $t_0 = 10^{-11}$  s. Using the same values, Fig. 2 shows how write delay scales with temperature and voltage for two values of activation energies. Note that though temperature is a function of voltage, it is still convenient to consider it as an independent parameter given broad range of temperature–voltage relations. From Fig. 2a,  $t_S = 100$  ns implies  $\sim 650$  K internal temperature at  $\sim 1$  V applied voltage. With  $U_F = 2$  eV, the endurance is of the order of 10,000 for this case. If write speed is increased by factor of 100, e.g., by applying 2 V and causing internal heating up to  $\sim 720$  K, the endurance is decreased accordingly to 100. For more robust devices, e.g., assuming  $U_F = 3$  eV and the same other parameters, the corresponding values of endurance are  $10^8$  and  $10^4$ , respectively.

Because of similar physics, the model can be applicable to flash memory devices. For example, results in Ref. [10] support the proposed tradeoff for flash memories with parameters in Eq. 5 close to the ones considered for memristive devices in the discussion above. In particular, Fig. 3 shows that exponent in Eq. 5 ranges from 1 to 2, while  $t_0$  parameter ranges from  $10^{-13}$  s to  $10^{-15}$  s for different types of oxides. The tradeoff might be also similar



**Fig. 3** Experimental data for rf-plasma-grown  $\text{AlO}_x$  barrier endurance as a function a voltage applied to the barrier, which is recalculated as a corresponding write time on x axis. Reproduced from Ref. [10]. The dashed lines are power law fitting using Eq. 5

for many other emerging nonvolatile memories based on phase-change [14], magnetoresistive, and ferroelectric materials [16], because of thermally activated nature of switching. For example, write kinetics was studied in phase-change memories [14] and it was shown that switching speed depends exponentially on the applied electric field and temperature [7].

It is worth noting that in memristors with filamentary switching, there exists at least one other possible mechanism which can lead to higher endurance with larger stresses, which is the opposite of the discussed tradeoff. In such memories, the smaller stress can in principle cause more unwanted lateral diffusion away from the filament relative to the useful (i.e., in terms of switching) drift along the filament. Understanding the importance of this effect as compared to the considered failure mechanisms will require more experimental and theoretical studies.

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