

# Optimized stateful material implication logic for three-dimensional data manipulation

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## ABSTRACT

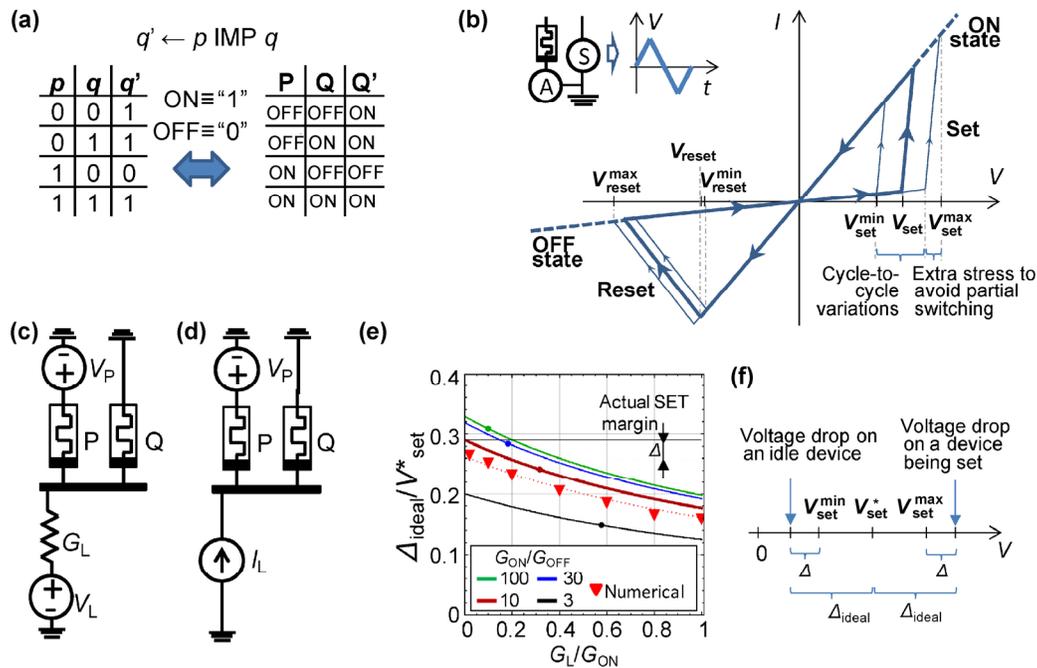
The monolithic three-dimensional integration of memory and logic circuits could dramatically improve the performance and energy efficiency of computing systems. Some conventional and emerging memories are suitable for vertical integration, including highly scalable metal-oxide resistive switching devices (“memristors”). However, the integration of logic circuits has proven to be much more challenging than expected. In this study, we demonstrated memory and logic functionality in a monolithic three-dimensional circuit by adapting the recently proposed memristor-based stateful material implication logic. By modifying the original circuit to increase its robustness to device imperfections, we experimentally showed, for the first time, a reliable multi-cycle multi-gate material implication logic operation and half-adder circuit within a three-dimensional stack of monolithically integrated memristors. Direct data manipulation in three dimensions enables extremely compact and high-throughput logic-in-memory computing and, remarkably, presents a viable solution for the Feynman Grand Challenge of implementing an 8-bit adder at the nanoscale.

## 1 Introduction

Material implication (IMP) is a universal Boolean logic (Fig. 1(a)) that is particularly suitable for implementing “stateful” logic circuits [1]. At the core of stateful logic are memory devices that serve the dual roles of performing computation and storing (latching) the results. The implementation with the greatest potential is based on highly scalable memristors [2–8]. In the simplest case, memristors are two-terminal devices,

whose conductance can be switched reversibly with relatively large (write) voltages, e.g., applying  $V \geq V_{\text{set}}$  to switch the device to the ON state, which is characterized by high conductance  $G_{\text{ON}}$ , and  $V \leq V_{\text{reset}}$  to switch it to the OFF state, which has low conductance  $G_{\text{OFF}}$  (Fig. 1(b)). The device’s conductance remains unchanged when relatively small (read) voltages are applied. Specifically, in one realization of memristor-based IMP logic, logic states “0” and “1” are encoded using the low and high conductive states of a memristor,

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**Figure 1** Memristor-based material implication logic. (a) Logic truth table and its mapping to memristor's states. (b) A sketch of simplified (linear)  $I-V$  switching curve for a memristor. The thick (thin) solid lines schematically show an  $I-V$  curve with average (maximum and minimum) set and reset thresholds. The inset shows the experimental setup. (c) Originally proposed [1] and (d) optimized IMP logic circuits with particular polarity of memristors. (Other possible configurations are shown in Fig. S6 in the ESM.) (e) The set margin as a function of the load conductance for several representative ON-to-OFF conductance ratios. For convenience, the margins and load conductances are normalized with respect to mid-range set voltages  $V_{set}^*$  and  $G_{ON}$ , respectively. The solid dots show the margins for the previously proposed optimal load conductance  $G_L^*$ , while the solid triangles are the margins that were obtained with numerical simulations using the fitted experimental device characteristics (shown in Fig. S4(b) in the ESM). The solid grey lines denote the maximum set margins, while the differences between the solid and dashed lines show the actual set margins when taking into account variations in the set threshold voltage extracted from the experimental data (shown in Fig. 3(b) inset). (f) A diagram showing the definition of margins in the context of set transition.

respectively. Using the divider circuit shown in Fig. 1(c),  $q' \leftarrow p \text{ IMP } q$  is an implication between logic variables  $q$  and  $p$ , stored in memristors  $Q$  and  $P$ , respectively, which is performed by applying specific "clock" voltage pulses  $V_P$  and  $V_L$ , so that the result of the computation is placed in  $Q$  as a new conductive state. Similar to other nonconventional computing approaches [9, 10], voltage pulses  $V_P$  and  $V_L$  are effectively clock signals that do not carry any information. Their amplitudes are fixed and are chosen according to the load conductance  $G_L$  and memristor parameters, e.g.,  $G_{ON}$ ,  $G_{OFF}$ ,  $V_{set}$  and  $V_{reset}$  for the ideal memristor without variations (Fig. 1(b)), such that device  $Q$  switches from the low to high conductive state only when device  $P$  is in the low conductive state.

The appealing feature of stateful logic is that the result of the logic operation is immediately latched.

Thus, IMP logic circuits based on non-volatile memristors are immune to power supply shortages, which could be advantageous in the context of energy scavenging applications. Even more importantly, stateful logic does not draw static power and enables very high throughput information processing because of the possibility of fine-grained pipelining. In many respects, stateful IMP logic is similar to other logic-in-memory computing approaches [9–13] that do not suffer from the memory bottleneck problem of conventional Von Neumann architectures [14]. Several theoretical studies have predicted a significantly higher performance and energy efficiency for memristor-based IMP logic circuits (and very similar concepts) compared to conventional approaches for high-throughput computing applications [15–22].

Although IMP logic has already been implemented

with a variety of memory devices [22–29], prohibitively large cycle-to-cycle and device-to-device variations in memristors have limited experimental demonstrations to simple gates with stand-alone devices and typically just a few cycles of operations. (In addition, for practical, large-scale IMP logic circuits, the sneak-path problem is expected to be another major challenge [30–34] (see Fig. S9 in the Electronic Supplementary Material (ESM)). Device variations reduce the allowed  $V_P$  and  $V_L$  voltage range within which correct operation is assured. In fact, IMP logic is more prone to variations, and a demonstration of memory functionality does not guarantee that the same circuit can be adapted for performing logic operations (section S3 in the ESM). Extending IMP logic to more promising three-dimensional circuits [4–7, 35, 36] is even more difficult, because more sophisticated fabrication processes and a higher integration density can further aggravate the device variation problems. The main goal of this study was to address these challenges and ultimately demonstrate robust stateful IMP logic in monolithic three-dimensional metal-oxide memristor structures.

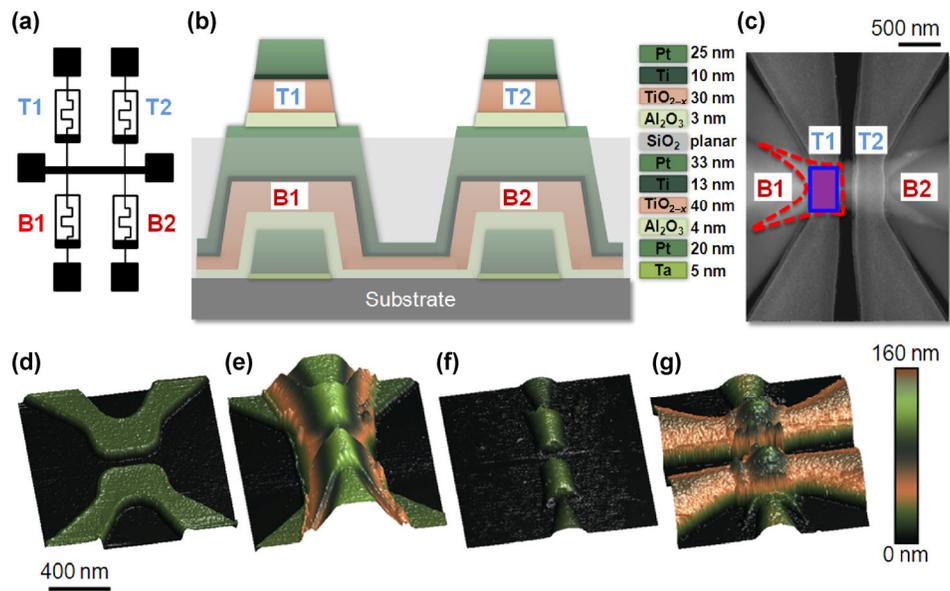
## 2 Theoretical and experimental

Significant switching voltage variations are a major challenge for implementing IMP logic. Therefore, it is natural to choose circuit parameters (i.e.,  $G_L$ ,  $V_L$  and  $V_P$ ) that maximize the range of variations (also referred as margins) that can be tolerated without comprising the correctness of the logic operation. Some earlier works suggested choosing  $G'_L = (G_{ON} \cdot G_{OFF})^{1/2}$  for the most optimal design [30, 37].

However, our analytical and numerical analyses of IMP logic operations (see section S3 in the ESM for details) showed that the set margins monotonically increased as the load conductance decreased (Figs. 1(e) and 1(f) and Fig. S7 in the ESM). The largest margins were found for  $G_L = 0$ , which could not be implemented with the original circuit, although it could easily be realized by replacing the load resistance and voltage source with a current source (Fig. 1(d)). The transition from the original circuit with the earlier suggested  $G'_L$  to the modified one with an optimized current source  $I_L$  increased the set margins by more than 20% (Fig. 1(e)).

The performance of this circuit was tested on a two-level stack with four metal-oxide memristors. Two memristors were fabricated in the bottom level, and two others were monolithically integrated directly above, with all of the devices sharing a common middle electrode (Figs. 2(a)–2(c)). The major steps involved in the fabrication were the patterning of the Ta/Pt bottom electrode using e-beam evaporation and lift-off, patterning of the bottom device's  $Al_2O_3/TiO_{2-x}$  layer and Ti/Pt middle electrode using reactive sputtering and lift-off, planarization by chemical mechanical polishing and the etch-back of the plasma-deposited sacrificial silicon oxide, and patterning of the top device's  $Al_2O_3/TiO_{2-x}$  layer and Ti/Pt top electrode by reactive sputtering and lift-off (Figs. 2(d)–2(g)). The device structure, oxide film thicknesses, and titanium oxide stoichiometry, which was controlled by changing the oxygen to argon flow ratio during sputtering, were selected based on our earlier study [38], with the primary objective of lowering the forming voltages and improving the uniformity of the switching characteristics.

In particular, thin Ti and Ta layers were deposited to improve the electrode adhesion. The addition of Ti to the middle and top electrodes also ensured ohmic interfaces with the titanium dioxide layer, which was important for the device's asymmetry [2, 39]. Low forming voltages reduced the electrical stress during electroforming [38], while *in-situ* contacts between the titanium oxide and the metal electrodes, which were fabricated without breaking the vacuum, ensured high-quality interfaces [40], with both factors essential for improving the uniformity of the memristor's switching characteristics. Furthermore, planarization reduced the middle electrode roughness, which resulted from the residual sidewall deposition and was critical for lowering the variations in top-level devices (Figs. S1–S3 in the ESM). The absence of an annealing step, which is typically used for fine-tuning the defect profile in metal oxide memristors [8, 38], and the low-temperature (<300 °C) budget during the fabrication, simplified the three-dimensional integration and made the fabrication process compatible with conventional semiconductor technology. More details about the fabrication are provided in section S1 in the ESM.



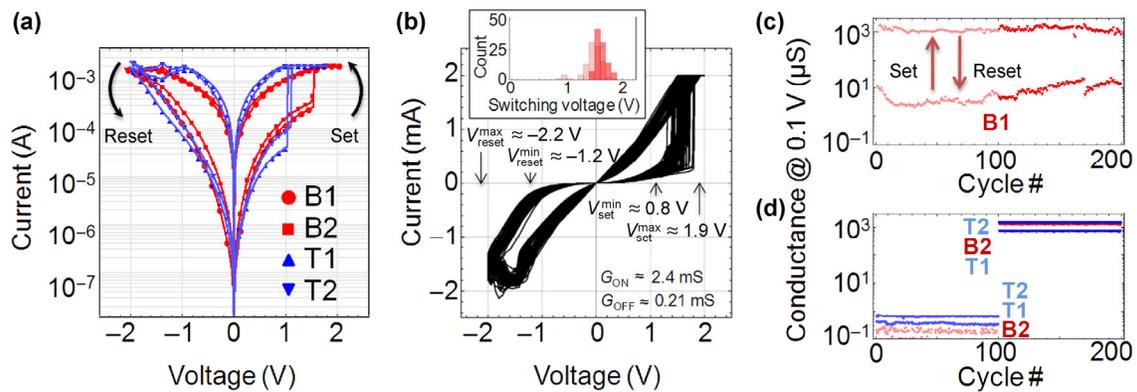
**Figure 2** Stacked  $\text{Al}_2\text{O}_3/\text{TiO}_{2-x}$  memristor circuit: fabrication details. (a) An equivalent circuit. B1 and B2 denote bottom devices, while T1 and T2 are the top ones. (b) A drawing of the device's cross-section showing the material layers and their corresponding thicknesses. (c) A top-view scanning-electron-microscope image of the circuit. The red, blue, and purple colors were added to highlight the locations of the bottom and top devices, and their overlap, respectively. (d) and (e) Top-view atomic-force-microscope images of the circuit during different stages of fabrication, in particular showing: (d) the bottom electrode, (e) middle electrode, (f) middle electrode after the planarization step, and (g) top electrode.

Figures 3(a) and 3(b) show typical memristor  $I$ - $V$  characteristics obtained by applying positive and negative quasi-direct current (DC) triangular voltage sweeps. The switching polarities of all the devices correspond to the bottom active interface, which is in agreement with the devices' asymmetric structure. For all the devices, the set switching was rather sharp, whereas the reset process was gradual. For example, the device B1 reset transition started at  $V_{\text{reset}}^{\text{min}} \approx -1.5$  V; however, to avoid partial switching, voltage exceeding  $V_{\text{reset}}^{\text{max}} \approx -2.2$  V had to be applied (Fig. 3(b)). A slightly thicker titanium dioxide layer for the bottom devices resulted in higher set threshold voltages compared to those of the top ones (Fig. 3(a) and Fig. S4 in the ESM). As Figs. 3(c) and 3(d) show, repetitive switching between the ON and OFF states of one device did not disturb the states of others, which suggested that the thermal crosstalk [41] was negligible in this system. The current ratios measured at 0.1 V between the ON and OFF states were well above one order of magnitude for all the memristors. Other characteristics such as the endurance and retention were close to those reported earlier for similar devices [37, 42].

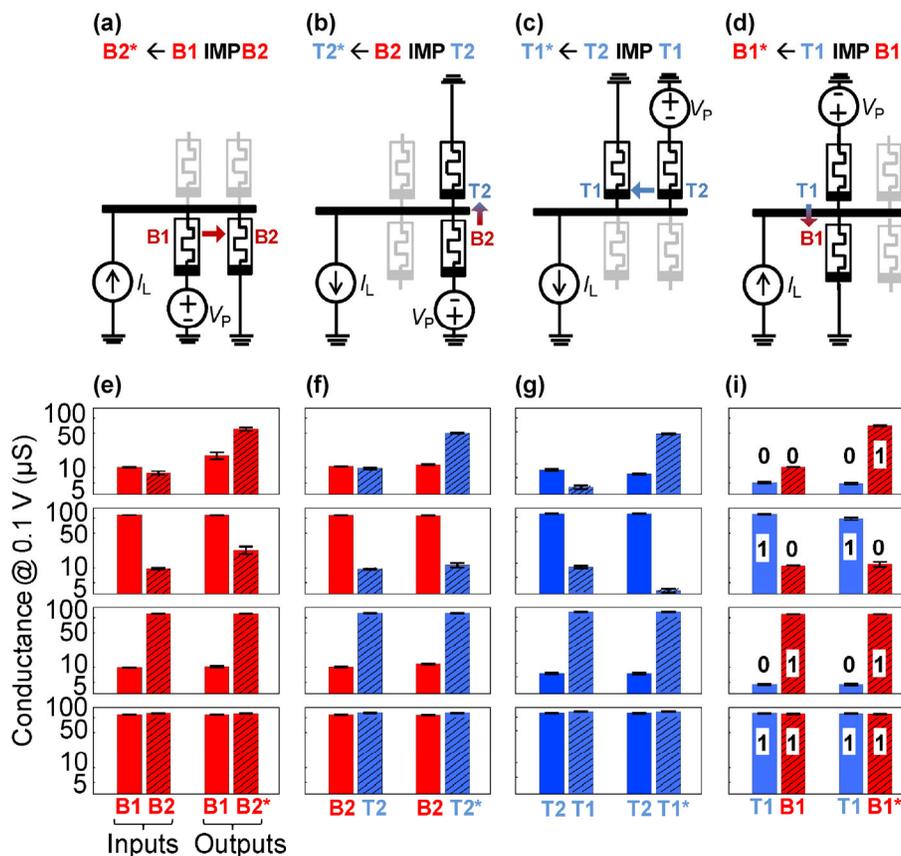
### 3 Results and discussion

Because the set threshold voltage variations were non-negligible (Fig. S5 in the ESM), the 20% boost in variation tolerance provided by the proposed circuit design was critical for our experiment. It should be noted that, in principle, IMP logic can also be implemented using a memristor's reset transition, i.e., assuming that logic states "0" and "1" are represented by the ON and OFF states instead. However, this would not be helpful in our case, because the gradual reset transition presents an even larger problem (see section S3.1 in the ESM for more details).

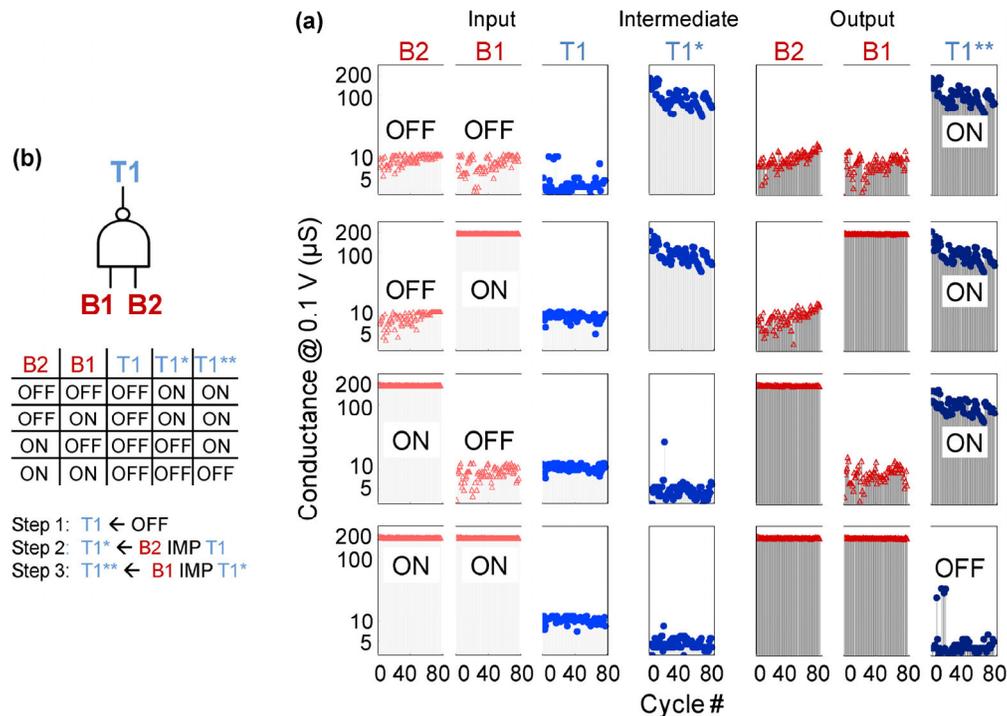
Using the variation tolerant design with optimal values of  $I_L$  and  $V_P$ , which were obtained from accurate numerical simulations based on experimental (nonlinear)  $I$ - $V$  curves, we successfully demonstrated IMP logic with the fabricated memristor circuit (Figs. 4 and 5, and Figs. S9 and S10 in the ESM). For simplicity, the current source used was the one provided by the source measurement unit (SMU) of the Agilent measurement equipment. In a hybrid complementary metal-oxide-semiconductor (CMOS)/memristor integrated circuit,



**Figure 3** Stacked  $\text{Al}_2\text{O}_3/\text{TiO}_{2-x}$  memristor circuit: electrical characterization. (a) Representative  $I$ - $V$  curves for all devices. (b) Switching  $I$ - $V$  curves showing 100 cycles of operation for device B2. The light and dark color histograms in the inset show the corresponding cycle-to-cycle  $V_{\text{set}}^{\text{min}}$  and  $V_{\text{set}}^{\text{max}}$  statistics. (c) Conductance of device B1 that was repeatedly switched 200 times and (d) those of the other three devices in the circuit that were kept in the OFF states for the first 100 cycles, and then in the ON states for the remaining 100 cycles. In all the experiments, the memristors were switched by applying triangular voltage pulses to the corresponding top terminal of the device.



**Figure 4** Three-dimensional data manipulation using optimized material implication logic circuit. (a)–(d) Circuit schematics and (e)–(i) corresponding experimental results showing device’s conductances before and after IMP operation implemented with various initial states and pairs of memristors in a circuit. In (e)–(i), each graph shows the averaged conductances and their standard deviations for 20 experiments. IMP logic was performed by biasing the corresponding device with  $V_p = 0.25$  V and applying a 10-ms  $I_L = 550$   $\mu\text{A}$  load current pulse for the cases in (a) and (d), i.e., when the result was written into the bottom device, and  $I_L = 200$   $\mu\text{A}$  when the output was one of the top devices ((b) and (c)).



**Figure 5** Three-dimensional NAND Boolean operation via optimized material implication logic. (a) Schematics and truth table showing intermediate steps. (b) Experimental results showing 80 cycles of operation with >93% yield for all four combinations of initial states. The initial states were set similar to those in the Fig. 4 experiments, while  $V_p = -0.15$  V, and the applied load current was a 10-ms pulse with  $I_L = -550$   $\mu\text{A}$ .

the physical implementation could be based on a circuit as simple as just one CMOS field effect transistor working in its saturation regime. In the first set of experiments, a series of IMP operations were performed sequentially utilizing four different pairs of memristors (Fig. 4 and Fig. S9 in the ESM). Before each logic operation, the devices were always written to the specified initial states. Therefore, this experiment provided proof of memory and logic functionality implemented within the same circuit. Moreover, the considered pairs constituted all of the possible combinations of the memristor's polarities in an IMP circuit and hence were sufficient to compute and move information in any direction within the circuit.

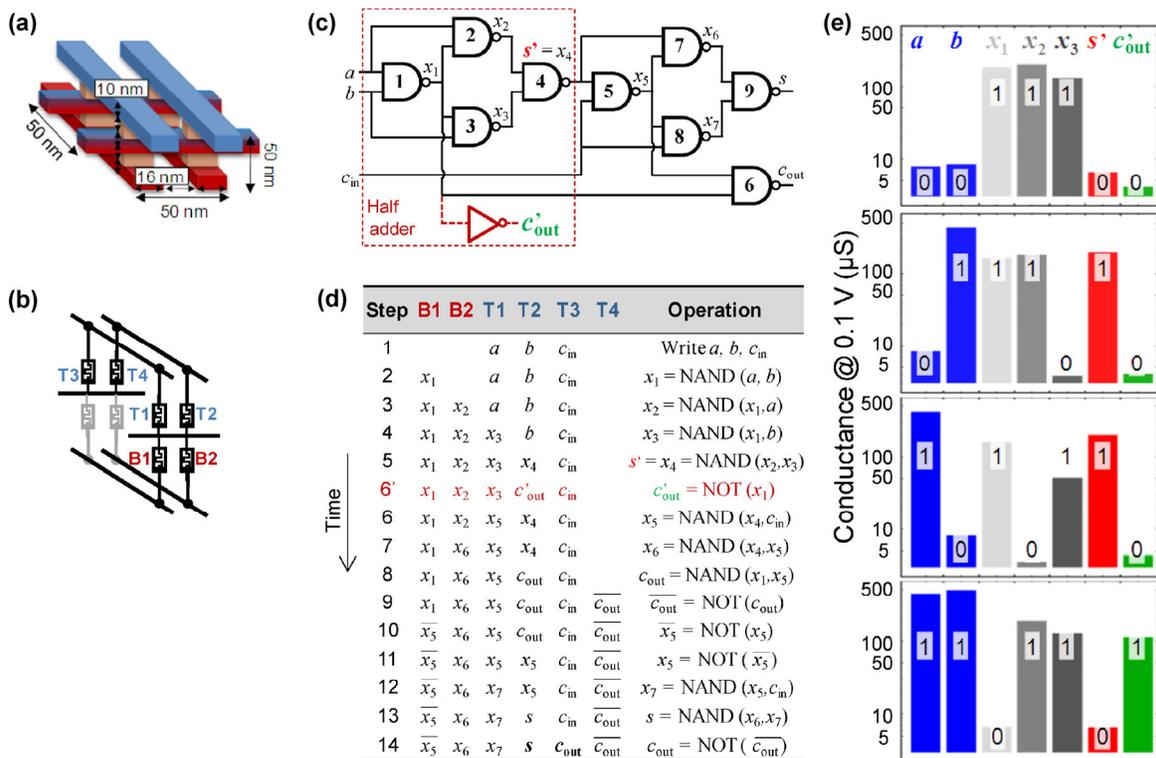
Normally, during the first experiment, the output conductances are close to the extreme ON and OFF values. Thus, it should be possible to cascade IMP logic gates, i.e., use the output of one gate as an input for another. To confirm this, in the next series of experiments, we implemented the NAND Boolean logic operation, for which the inputs were the states of the

bottom-level devices and the output was stored in one of the top-level memristors (Fig. 5 and Fig. S10 in the ESM). The NAND gate was realized in three steps: an unconditional reset, followed by two sequential IMP operations [1]. The result of the first IMP operation was stored in the top-level device, which was then used as one of the inputs to the second IMP gate. In some rare cases (~6.5% of the total IMP operations), there is some visible reduction in the ON-to-OFF conductance ratio. This is not desirable because the set margins decrease with the ON-to-OFF ratio (Fig. 1(e)). One plausible solution to restore the ratio is to read the state and write it back, i.e., similar to what was implemented in the first experiment. A better approach, which does not involve a read operation, is to apply a specific voltage pulse to the IMP logic circuit (see the experimental results on Figs. S11 and S12 and their discussion in section S4 in the ESM).

Interestingly, the approach based on 3D IMP logic enables a practical solution to one of the Feynman Grand Challenges—the implementation of an 8-bit adder that fits in a cube no larger than 50 nm in any

dimension [43]. The major building block—a full adder, which adds Boolean variables  $a$ ,  $b$ , and  $c_{in}$  to calculate the sum  $s$  and carry-out  $c_{out}$ , requires six memristors and consists of two monolithically stacked  $2 \times 2$  crossbars sharing the middle electrodes (Fig. 6(a)). Two of the memristors in the crossbar are assumed to be either not formed or always kept in the OFF state (Fig. 6(b)), which eliminates the typical leakage currents for crossbar circuits [30–34] and makes the IMP logic set margins similar to those of the demonstrated circuit. In particular, at the start of computation,  $a$ ,  $b$ , and  $c_{in}$  are written to the specific locations in the circuit (Fig. 6(c)). A sequence of NAND operations, each consisting of one unconditional reset step and two IMPs (Fig. 5), is then performed to compute  $c_{out}$  and  $s$  according to the particular implementation of Fig. 6(d). Occasional NOT operations are

implemented with one unconditional reset step and one IMP step and used to move variables within the circuit. In total, the full adder is implemented with nine NAND gates and four NOT gates, i.e., 13 unconditional reset steps and 22 IMP steps. The simplest way to read an output of an adder is to electrically measure the state of memristors T2 and T3 (Fig. 6(c)). Alternatively, the output can be sensed as a mechanical deformation of the upper metal electrodes, which is often observed in metal-oxide memristors [44] or using scanning Joule expansion microscopy [45]. A full 8-bit adder could be implemented in a ripple-carry style [46] by performing the full adder operation eight times. To verify that the proposed adder implementation is realistic, we experimentally demonstrated a half-adder circuit on a  $2 \times 2$  vertical stack of memristors (Fig. 6(e)). Such a half-adder implementation requires one NOT and



**Figure 6** Adder implementation with 3D IMP logic. (a) Drawing of a structure with dimensions satisfying Feynman Grand Challenge and (b) its equivalent circuit. (c) and (d) The sequence of steps and specific mapping of the logic variables to the circuit’s memristors for a particular implementation of the full/half adder shown in (d). In (d), steps 1 through 5 are common for the full and half adders. Step 6’ is only required for the half adder, while steps 6 through 14 are only used for the full adder. In addition, the last step for the full adder, in which  $c_{out}$  is placed in the same location as  $c_{in}$ , is only required to ensure a modular design, but might be omitted in more optimal implementations. (e) An experimental demonstration of a half adder implemented following steps 1 through 5 and step 6’ from (d).  $I_L = 800 \mu\text{A}$  and  $V_P = 0.6 \text{ V}$  were used to perform steps 2 and 3, while  $I_L = -375 \mu\text{A}$  and  $V_P = -0.3 \text{ V}$  were used for steps 4 and 5.

four NAND operations (Figs. 6(c) and 6(d)), i.e., about half of the complexity of a full adder implementation.

## 4 Conclusions

In summary, we demonstrated an optimized approach for logic-in-memory computing and proved its reliability by performing hundreds of cycles of three-dimensional data manipulation in monolithically integrated circuits. As the rapid progress of memristor technology continues, it will eventually become sufficiently advanced to enable large-scale integration of memristive devices with sub-nanosecond, pico-Joule switching capable of enduring  $> 10^{14}$  cycles with high nonlinearity, which has already been demonstrated for discrete devices [2, 3]. As a result, we expect that the presented approach will become attractive for high-throughput and memory-bound computing applications suffering from memory bottleneck problems. Furthermore, we showed how the presented approach establishes a realistic pathway toward resolving one of the Feynman Grand Challenges. The remaining challenge is to scale down the circuitry (Fig. 6(a)), which does not seem to be an unrealistic task given that discrete metal-oxide memristors with similar dimensions [8, 47] and much more complex (but less dense) memristive circuits [4, 5, 7, 38] have already been demonstrated.

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**Electronic Supplementary Material:** Supplementary material (further details of the fabrication and electrical testing procedures, theoretical optimization of the circuit for the material implication logic, and three-dimensional data manipulation experiments) is available in the online version of this article at <http://dx.doi.org/10.1007/s12274-016-1260-1>.

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## Electronic Supplementary Material

# Optimized stateful material implication logic for three-dimensional data manipulation

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### S1 Circuit fabrication

Devices were fabricated on a Si wafer coated with 200 nm thermal SiO<sub>2</sub>. Circuit fabrication involved four lithography steps using ASML S500/300 DUV stepper with a 248 nm laser. To prevent misalignment of device layers, the bottom devices were made larger with an active area of 500 nm × 500 nm, as compared to 300 nm × 500 nm active area of top devices.

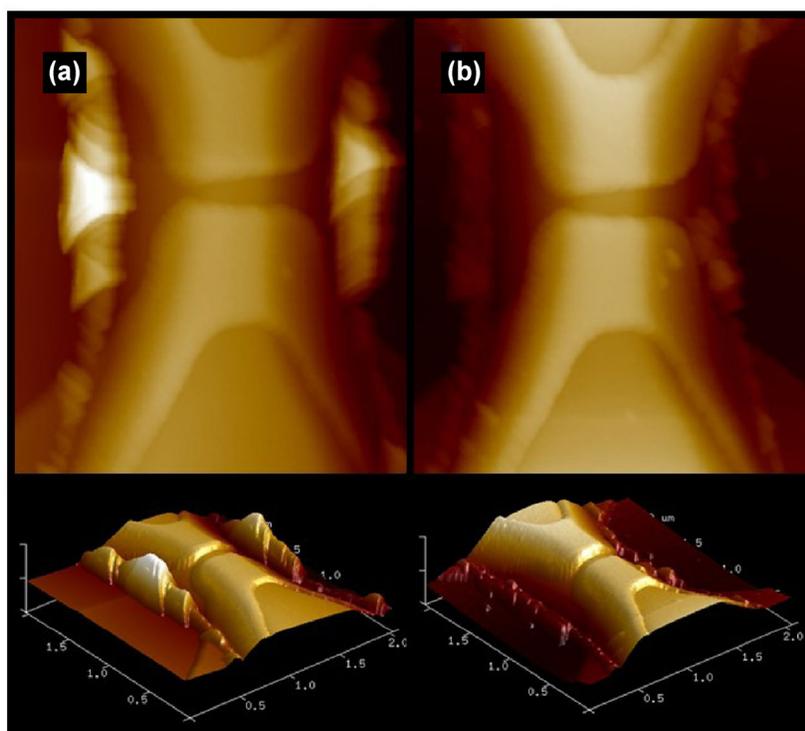
In particular, in the first lithography step the bottom electrode was patterned using a developable antireflective coating (DSK-101-307 from Brewer Science, spin speed 2,500 rpm, bake 185 °C, thickness ~50 nm) and positive photoresist (UV210-0.3 from Dow, spin speed 2,500 rpm, bake 135 °C, thickness ~300 nm). 5 nm/20 nm of Ta/Pt were evaporated at 0.7 Å/s deposition rate in a thin film metal e-beam evaporator. After the liftoff, a “descum” by active oxygen dry etching at 200 °C for 5 min was performed to remove photoresist traces.

In the next lithography step, the middle electrode was patterned and the bottom device layer (4 nm/40 nm of Al<sub>2</sub>O<sub>3</sub>/TiO<sub>2-x</sub> bi-layer) and middle electrode (13 nm/33 nm of Ti/Pt) were deposited using low temperature (<300 °C) reactive sputtering in an AJA ATC 2200-V sputter system. To minimize sidewall redeposition on the photoresist, which was undercut during sputtering of the middle electrode and caused “bunny-ear” formation around the edges of middle electrode (Fig. S1(a)), both metals were deposited at 0.9 mTorr, which is the minimum pressure needed to maintain plasma in the sputtering chamber. Also, the thickness of the photoresist undercut layer was optimized to provide more shadowing by using a liftoff layer of LOL2000 (from Shipley Microposit, spin speed 3,500 rpm, bake 210 °C, thickness ~200 nm) followed by the same DSK101/UV210 stack as for the first lithography step mentioned above. Occasional lumps were reduced to the height of ~20–30 nm by swabbing in isopropanol (Fig. S1(b)).

Severe topography of the bottom level devices (Fig. 2(e)) may cause shorts and large variations in top level devices. To overcome this problem, a planarization step was performed using chemical mechanical polishing and etch-back of 750 nm of sacrificial SiO<sub>2</sub>. SiO<sub>2</sub> served the double purpose: as a sacrificial material for planarization

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and as an insulation among devices. The most optimal planarization was achieved by depositing SiO<sub>2</sub> at 175 °C using the PECVD method. Following the deposition, 400 nm of SiO<sub>2</sub> were removed by chemical mechanical polishing for 3 min achieving surface roughness of less than 1 nm. The last step in planarization procedure was to etch back ~250 nm of SiO<sub>2</sub> until the middle electrodes were exposed (Fig. 2(f)). Several etch-back approaches were investigated with the best results achieved using CHF<sub>3</sub> at 50 W, which had an etch rate of 0.2 nm/s (Fig. S2). In particular, the dry-etching with CHF<sub>3</sub> was done in steps to ensure < 5 nm roughness in the exposed middle electrode. AFM scans were performed after each etching step to check the thickness of the exposed electrode (Fig. S3) and to confirm that the post-etch surface has no traces of bunny-ear formations.

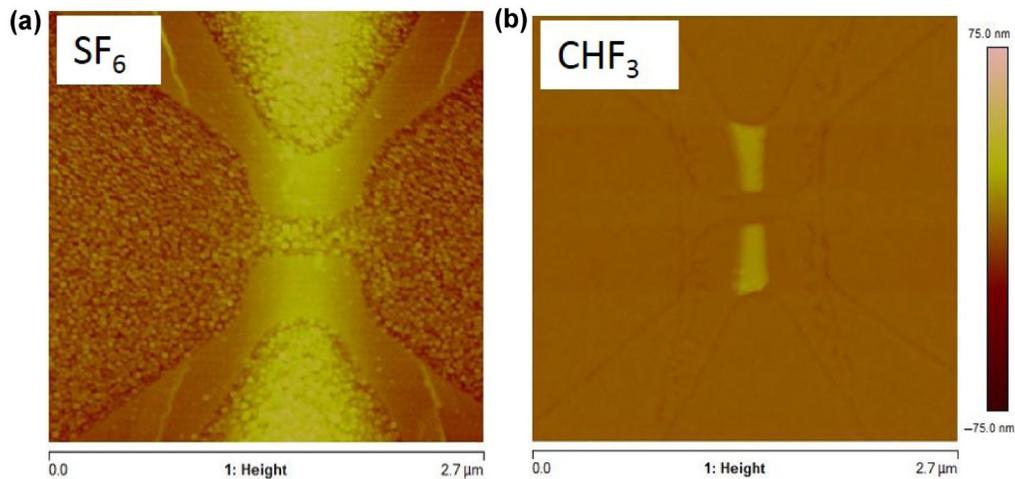


**Figure S1** Middle electrode topology due to sidewall redeposition during sputtering (a) using standard process which results in > 200 nm lumps at the edges of the electrode and (b) after deposition optimization and swabbing method, which allows reduction of lumps to 20–30 nm.

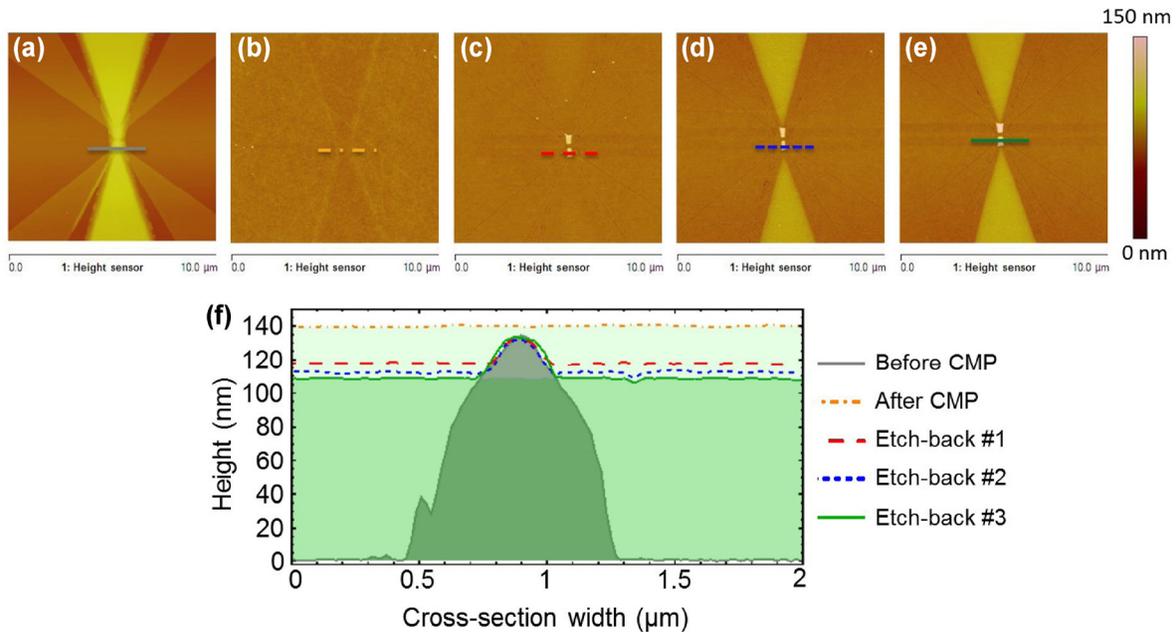
After planarization and partial middle electrode exposure, the top layer devices were completed by *in-situ* reactive sputtering of the switching layer, which consisted of 3 nm/30 nm of Al<sub>2</sub>O<sub>3</sub>/TiO<sub>2-x</sub> and Ti (10 nm)/Pt (25 nm) top electrode over patterned photoresist (DSK101/UV210).

Lastly, the pads of the bottom and middle electrodes were exposed through a CHF<sub>3</sub> etch of the sacrificial SiO<sub>2</sub> which was used for planarization.

In all lithography steps, the photoresist was stripped in the 1165 solvent (from Shipley Microposit) for 24 h at 80 °C.



**Figure S2** Comparison of two etch back methods for  $\text{SiO}_2$ . (a)  $\text{SF}_6$  achieving quadratic mean surface roughness  $> 6$  nm and (b)  $\text{CHF}_3$  with roughness less than 1 nm.

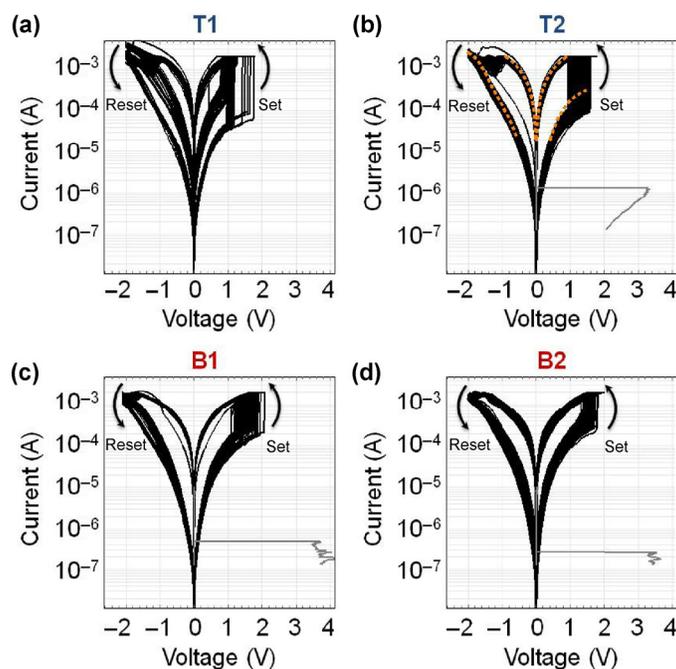


**Figure S3** A top-view AFM images of the circuit during different stages of planarization, in particular showing: (a) bottom device before planarization; (b) after chemical-mechanical polishing of  $\text{SiO}_2$  deposited over bottom device; (c) after etch #1 using  $\text{CHF}_3$  for 1,200 s showing partially exposed 18-nm-high middle electrode; (d) after etch #2 using  $\text{CHF}_3$  for 20 s showing partially exposed 22-nm-high middle electrode; (e) after etch #3 using  $\text{CHF}_3$  for 20 s showing partially exposed 28-nm-high middle electrode. (f) AFM height profiles taken across middle portion of the device (see marks on (a)–(e)) at the different planarization stages.

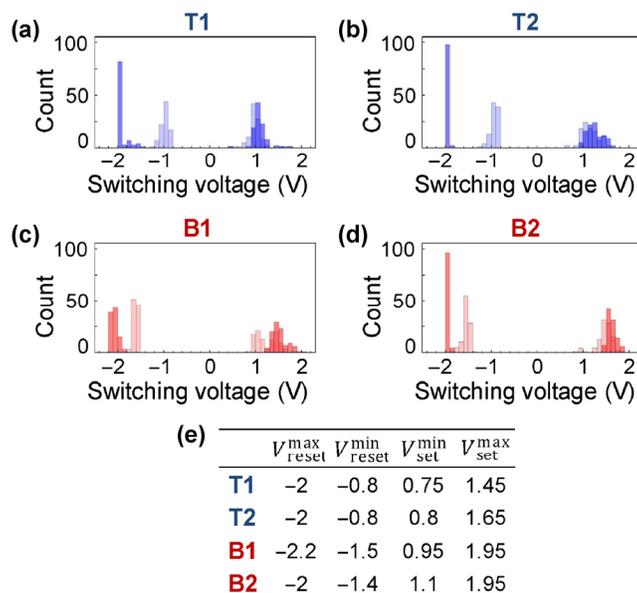
## S2 Electrical testing and device forming

All electrical testing was performed with an Agilent B1500 tool. The memristors were electroformed by grounding the device's bottom electrode and applying a current-controlled quasi-DC ramp-up to the device's top electrode, while keeping all other circuit terminals floating. For most of the devices forming voltages were around  $\sim 2$ – $3$  V, while device T1 did not require forming (Fig. S4). To minimize current leakage during the forming process, each memristor was switched to the OFF state immediately after forming.

For all devices the most severe are cycle-to-cycle variations in set voltage threshold (Fig. S5), which range from 0.7 to 1.6 V for the top layer devices, and from 1.1 to 1.9 V for the bottom ones. However, because of gradual switching,  $|V^{\max} - V^{\min}|$  statistics is comparable or wider for reset transition (Fig. S5).



**Figure S4** (a)–(d)  $I$ – $V$  curves showing 100 cycles of switching for all devices. Gray lines show current-controlled forming  $I$ – $V$  curves. The dashed orange curve on (b) is a fitting used for the numerical simulations (see section S3.2 below). For all cases, the  $I$ – $V$  switching curves were obtained by applying quasi-DC triangular voltage sweep to the corresponding top terminal of the device.



**Figure S5** Switching voltages statistics extracted from experimental results shown on Fig. S4 for (a) T1, (b) T2, (c) B1, and (d) B2 devices. On all panels, light and dark colors show the  $V^{\min}$  and  $V^{\max}$  voltage distributions, correspondingly, for set and reset transitions. For the set transition, the switching occurs as sequence of abrupt changes in current and  $V^{\min}$  ( $V^{\max}$ ) is defined as the voltage of the first (last) abrupt change. The reset transition is more gradual and here  $V^{\min}$  ( $V^{\max}$ ) is calculated as the voltage at which the change in  $I$ – $V$  curvature is the largest (smallest) near the offset (end) of switching. (e) Table summarizing key parameters.

### S3 Material implication logic

#### S3.1 Two device case—analytical method

The optimal circuit parameters  $V_P$ ,  $V_L$  and  $G_L$ , which result in the largest set margins could be derived analytically for the memristors with idealized linear  $I$ - $V$  curves (Fig. 1(b)). Let us first consider an IMP circuit with specific “parallel” configuration of memristors (Figs. 1(c) and S6(a)). Device Q is assumed to be the device switching and retaining the result of the implication logic operation. Device P serves as an enabling device allowing for the voltage drop on Q to be modulated according to its state and therefore, facilitating the conditional switching of Q to the ON state only when both Q and P are OFF. While device Q is switching, the device P should not be perturbed since the device Q switching is dependent on the memristance value of P. Assuming for convenience that  $V_Q = 0$ , the proper operation of the material implication logic circuit shown on Figs. 1(a) and 1(c) require that device Q is set only when both P and Q are in the OFF state and in all the other cases, both devices P and Q should be under non perturbing conditions, i.e.

$$-V_C|_{P=OFF, Q=OFF} \geq V_{set}^{max} \tag{S1}$$

$$-V_C|_{OTHERS} < V_{set}^{min} \tag{S2}$$

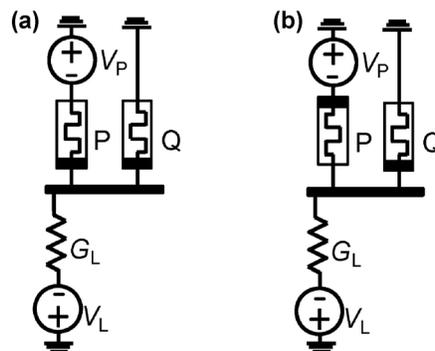
where

$$V_C = \frac{G_L V_L + G_P V_P}{G_L + G_P + G_Q} \tag{S3}$$

is a voltage on the common electrode. Device P should not be disturbed during the IMP operation, i.e.

$$(V_P - V_C)|_{ANY} < V_{set}^{min} \tag{S4}$$

$$(V_P - V_C)|_{ANY} > V_{reset}^{min} \tag{S5}$$



**Figure S6** (a) Parallel and (b) anti-parallel polarity configuration for memristor-based IMP logic.

Equations (S1), (S2), (S4), and (S5) define 12 inequalities in total. To eliminate redundant inequalities, let us first note that  $V_L \geq 0$  does not have valid solutions, while  $V_P \geq 0$  always results in sub-optimal margins. Assuming  $V_P < 0$  and  $V_L < 0$  and that memristors P and Q are characterized by the same parameters  $V_{set}^{min}$ ,  $V_{set}^{max}$ ,  $V_{reset}^{min}$ ,  $V_{reset}^{max}$ ,  $G_{ON}$ ,  $G_{OFF}$  (a more general case is discussed later) only three conditions must be considered, namely:

- voltage drop on device Q, when Q and P are in the OFF states, is larger than  $V_{set}^{max}$ ,
- voltage drop on device Q, when Q and P are in the ON and OFF states, respectively, is smaller than  $V_{set}^{min}$ , and
- voltage drop on device P, when Q and P are in the OFF states, is smaller than  $V_{set}^{min}$ .

Therefore, the largest set margins and the corresponding optimal parameters can be found by solving the following equations

$$\frac{-V_P G_{\text{OFF}} - V_L G_L}{2G_{\text{OFF}} + G_L} = V_{\text{set}}^* + \Delta_{\text{ideal}} \quad (\text{S6})$$

$$\frac{-V_P G_{\text{ON}} - V_L G_L}{G_{\text{OFF}} + G_{\text{ON}} + G_L} = V_{\text{set}}^* - \Delta_{\text{ideal}} \quad (\text{S7})$$

$$\frac{V_P(G_{\text{ON}} + G_L) - V_L G_L}{2G_{\text{OFF}} + G_L} = V_{\text{set}}^* - \Delta_{\text{ideal}} \quad (\text{S8})$$

where

$$V_{\text{set}}^* = (V_{\text{set}}^{\text{max}} + V_{\text{set}}^{\text{min}}) / 2 \quad (\text{S9})$$

Here,  $\Delta_{\text{ideal}}$  is a set margin for the binary zero-variations (i.e. ideal for the considered application) memristors for which  $V_{\text{set}}^* = V_{\text{set}}^{\text{max}} = V_{\text{set}}^{\text{min}}$ . Accounting for variations in set switching threshold and analog switching, a more relevant for our case margin is

$$\Delta = \Delta_{\text{ideal}} - (V_{\text{set}}^{\text{max}} - V_{\text{set}}^{\text{min}}) / 2 \quad (\text{S10})$$

From Eqs. (S7)–(S9)  $V_P$ ,  $V_L$  and  $\Delta_{\text{ideal}}$  are

$$\Delta_{\text{ideal}} = V_{\text{set}}^* \frac{G_{\text{ON}} - G_{\text{OFF}}}{2G_L + 3G_{\text{ON}} + G_{\text{OFF}}} \quad (\text{S11})$$

$$V_P = -2\Delta_{\text{ideal}} \quad (\text{S12})$$

$$V_L = -2V_{\text{set}}^* \frac{G_L^2 + 2G_L(G_{\text{ON}} + G_{\text{OFF}}) + G_{\text{OFF}}(3G_{\text{ON}} + G_{\text{OFF}})}{G_L(2G_L + 3G_{\text{ON}} + G_{\text{OFF}})} \quad (\text{S13})$$

According to Eq. (S10)  $\Delta_{\text{ideal}}$  is monotonically decreasing with  $G_L$  (Fig. 1(e)) and the maximum margins are achieved for  $G_L = 0$ , i.e. a circuit on Fig. 1(d) for which

$$\Delta_{\text{ideal}} = V_{\text{set}}^* \frac{G_{\text{ON}} / G_{\text{OFF}} - 1}{3G_{\text{ON}} / G_{\text{OFF}} + 1} \quad (\text{S14})$$

$$I_L = V_L G_L = -2V_{\text{set}}^* G_{\text{OFF}} \quad (\text{S15})$$

For devices with large ON-to-OFF conductance ratio, Eq. (S13) can be approximated with very simple formula

$$\Delta_{\text{ideal}} \approx V_{\text{set}}^* / 3 \quad (\text{S16})$$

It is instructive to compare IMP logic margins with those of passive crossbar memories. For example, let us consider the most optimal  $V/3$ -basing scheme [S1], and assume that voltages  $V$  and  $0$  are applied on the lines leading to the selected device, and  $V/3$ , and  $2V/3$  on the corresponding lines leading to the remaining devices. Assuming that voltage across the selected device is  $V = V_{\text{set}}^* + \Delta_{\text{memory}}$ , while it is  $V/3 = V_{\text{set}}^* - \Delta_{\text{memory}}$  across all other devices, it is straightforward to show that the margins for crossbar memory are

$$\Delta_{\text{memory}} = V_{\text{set}}^* / 2 \quad (\text{S17})$$

Thus voltage margins for memory circuits are more relaxed as compared to those of IMP logic. In principle, a somewhat larger IMP logic set margins can be obtained by not enforcing full switching, e.g. by defining  $V_{\text{set}}^{\text{max}}$  as the largest set threshold voltage due to cycle-to-cycle variations. However, in this case, the ON-to-OFF ratio will get reduced with every IMP logic operation, which is not desirable.

The analysis above is for a specific IMP logic based on memristors with identical linear static  $I$ - $V$  characteristics. It is straightforward to extend it to a more general case by using specific to memristors  $Q$  and  $P$  parameters in Eqs. (S6)–(S8), such as different set and reset threshold voltages for the top and bottom devices, which is the case relevant to the implemented circuit. For example, a more general set of equations for parallel configuration shown on Fig. S6(a), which is more convenient to solve for  $\Delta$  directly, is

$$\frac{-V_P G_{\text{OFF}} - V_L G_L}{2G_{\text{OFF}} + G_L} = V_{Q\text{set}}^{\text{max}} + \Delta, \quad \frac{-V_P G_{\text{ON}} - V_L G_L}{G_{\text{OFF}} + G_{\text{ON}} + G_L} = V_{Q\text{set}}^{\text{min}} - \Delta, \quad \frac{V_P (G_{\text{ON}} + G_L) - V_L G_L}{2G_{\text{OFF}} + G_L} = V_{P\text{set}}^{\text{min}} - \Delta \quad (\text{S18})$$

from which the actual margin for  $G_L = 0$  is

$$\Delta = \frac{(G_{\text{ON}} + G_{\text{OFF}})(V_{Q\text{set}}^{\text{min}} - V_{Q\text{set}}^{\text{max}}) + (G_{\text{ON}} - G_{\text{OFF}})V_{P\text{set}}^{\text{min}}}{3G_{\text{ON}} + G_{\text{OFF}}} \quad (\text{S19})$$

For anti-parallel configuration shown on Fig. S6(b), the set of equation is

$$\frac{-V_P G_{\text{OFF}} - V_L G_L}{2G_{\text{OFF}} + G_L} = V_{Q\text{set}}^{\text{max}} + \Delta, \quad \frac{-V_P G_{\text{ON}} - V_L G_L}{G_{\text{OFF}} + G_{\text{ON}} + G_L} = V_{Q\text{set}}^{\text{min}} - \Delta, \quad \frac{V_P (G_{\text{ON}} + G_L) - V_L G_L}{2G_{\text{OFF}} + G_L} = -(V_{P\text{set}}^{\text{min}} - \Delta) \quad (\text{S20})$$

and the actual margin for  $G_L = 0$  is

$$\Delta^{\text{anti}} = \frac{(G_{\text{ON}} + G_{\text{OFF}})(V_{Q\text{set}}^{\text{min}} - V_{Q\text{set}}^{\text{max}}) - (G_{\text{ON}} - G_{\text{OFF}})V_{P\text{reset}}^{\text{min}}}{3G_{\text{ON}} + G_{\text{OFF}}} \quad (\text{S21})$$

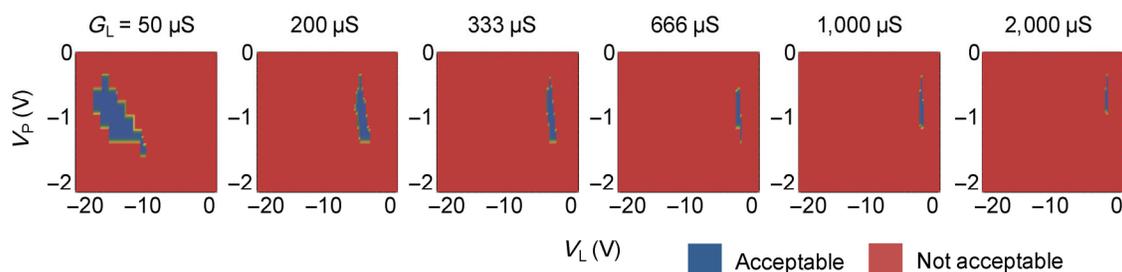
Because  $-V_{\text{reset}}^{\text{min}} > V_{\text{set}}^{\text{min}}$  typically holds for the considered devices (Fig. S5), from Eqs. (S19) and (S21) margins for parallel case are smaller, which is why this case is considered more in detail. Margins and optimal parameters for the remaining parallel (Fig. 4(a)) and antiparallel configurations (Fig. 4(d)) that were experimentally demonstrated, are similar to those described above with the only difference is that the signs for  $V_P$  and  $I_L$  are negative.

### S3.2 Two device case—numerical method

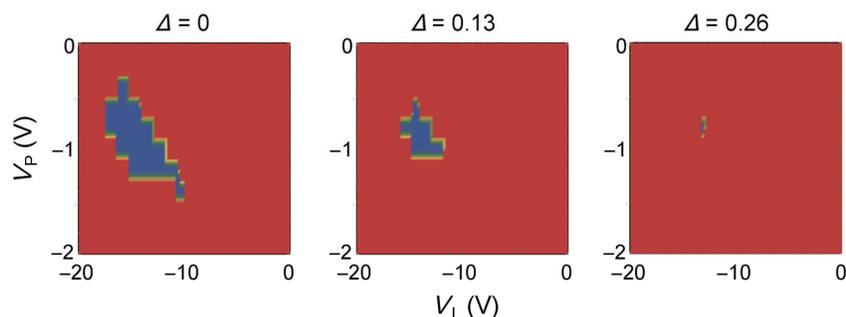
The analytical approach can be also utilized for IMP logic based on the memristors with more realistic nonlinear static  $I$ - $V$  by using  $G_{\text{ON}}$  and  $G_{\text{OFF}}$  measured at large (close to switching threshold) voltages. A more accurate approach, however, is to solve the 16 inequalities given by Eqs. (S1)–(S5) numerically. By fitting experimental  $I$ - $V$  curves (Fig. S4(b)) and using Mathematica's Newton–Raphson-based solver, we have obtained more accurate optimal values for  $V_P$  and  $V_L$ , which were used in experimental work. The fitting was done on log–log data using a polynomial function of 7th degree. The fitting function shows a good fit with  $R_2 > 0.999$  and is forced to pass through zero, since the current should be zero if the applied voltage is zero. The solver has 99.97% convergence for 22,000 generated points. The 6 points that did not converge in 100 iterations were discarded.

Graphical plots were derived showing acceptable ranges of  $V_P$  and  $V_L$  for various  $G_L$ s in the case of ideal devices requiring zero conditional switching margin to variations. The area of acceptable voltages increases as the  $G_L$  decreases (Fig. S7) confirming the analytical results. By introducing a non-zero switching margin term in

the constrains, the area of the acceptable region decreases. The highest value of margin for a particular  $G_L$  is considered the value at which the acceptable region vanishes in the graph (Fig. S8). This last acceptable point provides the optimal values for  $V_P$  and  $V_L$ . The margins calculated from numerical simulations for a specific IMP logic are shown on Fig. 1(e) and are in fairly good agreement with simple analytical model for a system with an ON-to-OFF conductance ratio of  $\sim 10$ . A step of 0.01 V was used which limits the accuracy of the numerical method.



**Figure S7** The area of acceptable voltages increases with decreasing  $G_L$ .



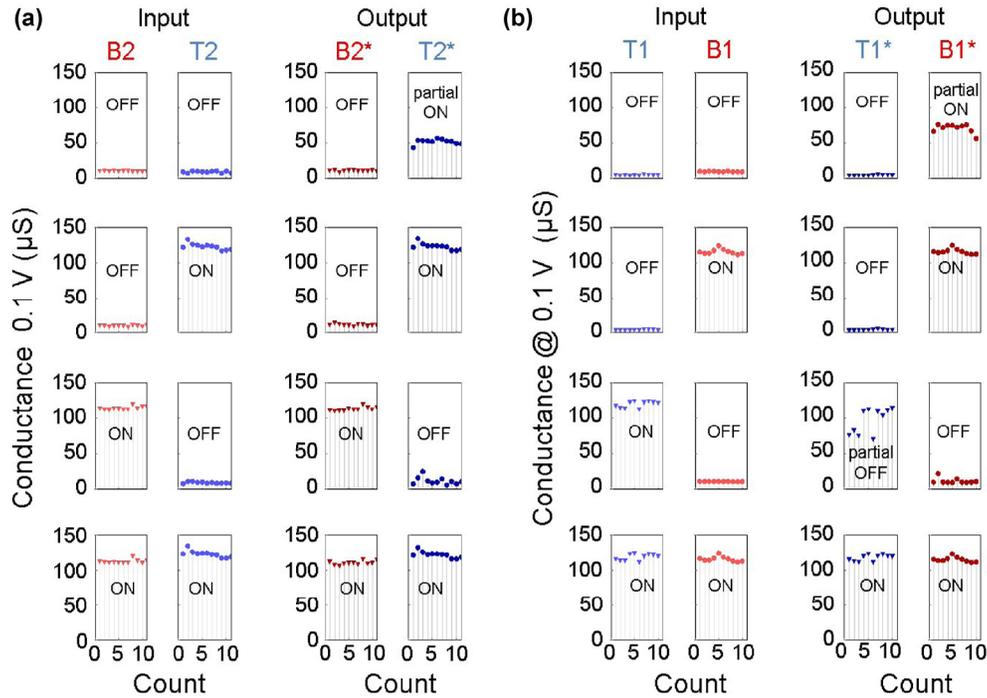
**Figure S8** The area of acceptable voltages decreases with increasing margin required ( $G_L = 50 \mu\text{S}$ ).

## S4 Material implication logic experiments

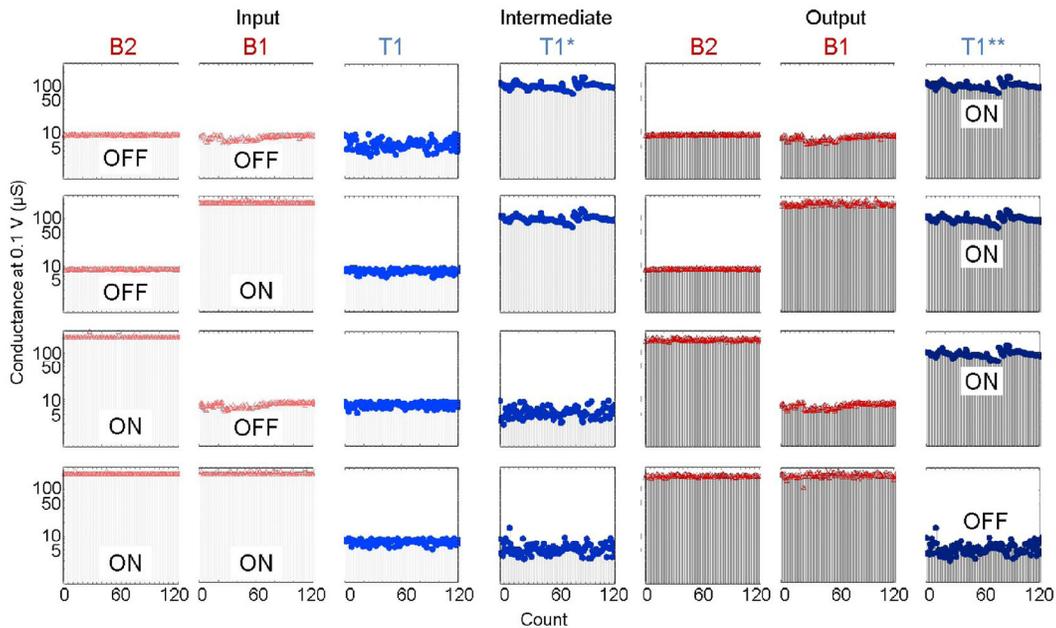
In all experiments, the current source was implemented by applying a current pulse of specific duration and amplitude using a Agilent B1500A semiconductor device parameter analyser. An Agilent 5250A low-leakage switch matrix was used to automatically reconfigure the connections between devices and source-measurement units (SMUs). Both the device parameter analyzer and the switch matrix were controlled using a computer with custom C++ code via a GPIB connection.

For IMP and NAND experiments presented in Figs. 4 and 5, the memristors were set to the initial states using a simplified version of the state tuning algorithm [S2] to ensure ON state above  $115 \mu\text{S}$  and OFF state below  $10 \mu\text{S}$ . In particular, a train of 1-ms pulses with increasing amplitude, starting from 0.5 V to maximum of 1.9 V with 0.1 V steps for reset pulses, and from 50 to 900  $\mu\text{A}$  with 50  $\mu\text{A}$  step for set pulses which resulted in initial state ON and OFF conductances measured at 0.1 V to be always close to 115, 115, 125, 120 and 10  $\mu\text{S}$ , 10, 5, 8  $\mu\text{S}$  for B1, B2, T1, and T2 devices, correspondingly. The optimal  $V_P$  and  $V_L$  were determined from numerical simulations with an additional constraint of using the same circuit parameters when the IMP logic output is in the bottom or top memristors. Such an additional constraint is representative of more general case when parameters of biasing circuitry are not chosen based on switching characteristics of individual memristors. Figure S9 shows additional information for the experiment presented in Fig. 4, while Fig. S10 shows experimental results for NAND operation obtained similarly to those shown on Fig. 5 using different stack of  $2 \times 2$  devices.

To ensure better set margins for the material implication logic in the half-adder experiment (Figs. 6(c)–6(e)), the initial memristor ON and OFF state conductances were set to  $\sim 500$  and  $\sim 5 \mu\text{S}$ , respectively, using the same modified tuning algorithm described above. After performing NAND operation to compute intermediate states  $x_1$ ,  $x_2$ , and  $x_3$ , the ON state sometimes dropped to  $50 \mu\text{S}$ . To prevent further set margins degradation, the conductances for intermediate states  $x_1$ ,  $x_2$ , and  $x_3$  were unconditionally restored to the highest values (Fig. S12).

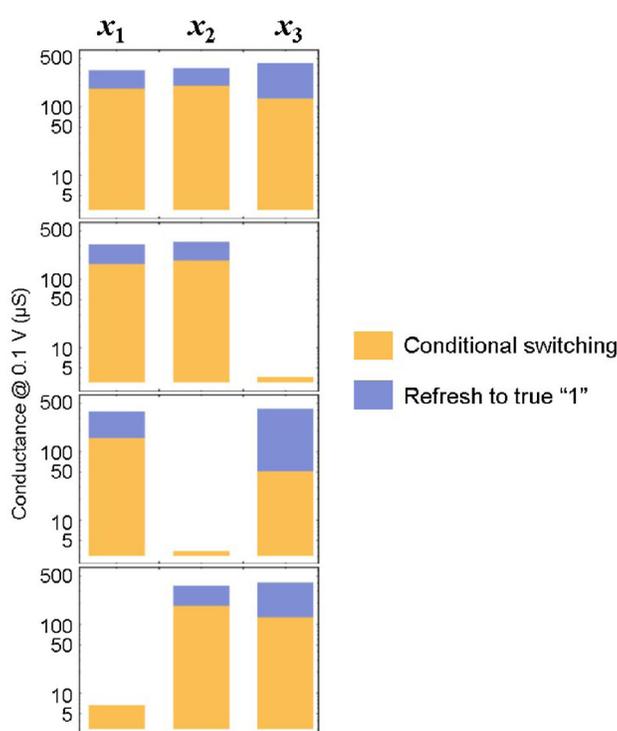


**Figure S9** 10 representative cycles for (a)  $T2^* \leftarrow B2 \text{ IMP } T2$  and (b)  $T1^* \leftarrow B1 \text{ IMP } T1$ .



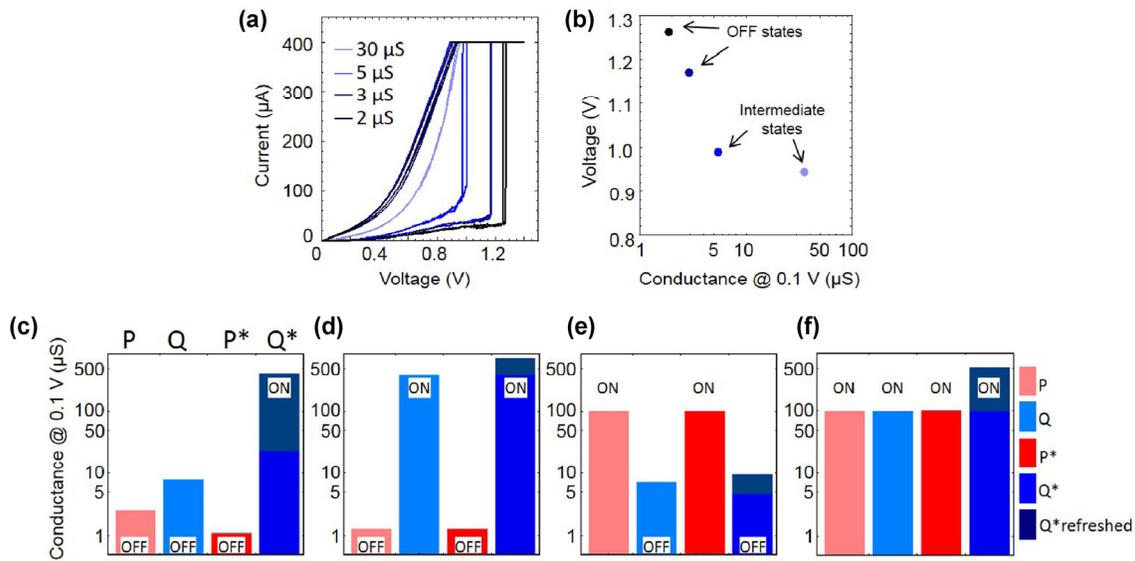
**Figure S10** Experimental results showing 120 cycles of operation for NAND Boolean operation via material implication logic.

In particular, one approach to recover from partial switching is to perform a sequence of read and write-back operations similar to the memory refresh performed in dynamic random access memories. However, this scheme would incur large overhead, i.e. in area in case the extra circuitry is used for refreshing multiple devices simultaneously, or in speed in case of sequential refresh operation. Here, we implemented an alternative scheme to recover from partial ON state which requires application of one common “refresh clock” voltage pulse for all the devices, without any need for state read-out (Fig. S11). Specifically, the idea is to utilize the particular dependence of set voltage on the initial state of the device (Fig. S12(a) and S12(b)). As shown in Fig. S12(b), refresh pulse amplitude can be chosen such that intermediate-state devices would be always switched to a more conductive ON state, while devices in the OFF state would remain undisturbed. To further verify this idea, Figs. S12(c)–S12(f) show successful refresh operation applied immediately after IMP logic using a 1 s 0.9 V voltage pulse.



**Figure S11** The conductance states before and after unconditional refresh operation.

It is worth noting that recently Breuer et al. [S3] experimentally demonstrated adder functionality using an approach, which is somewhat similar to the original material implication logic [S4]. The main drawback of that work, which makes it hardly practical [S5] and certainly inappropriate for Feynman challenge, is that implementing simple logic operations requires extensive processing outside of the memristor array—e.g., reading the output resistance and transforming it into the corresponding voltage after each computation. This is unlike our presented approach (and original material implication logic implementation) where the external circuit only generates a “clock” signal, which does not carry any information and which is used to perform both computation and refresh operation.



**Figure S12** (a)  $I$ - $V$  curves showing set switching for different initial states (measured at 0.1 V) when applying voltage sweep and (b) the extracted relationship between the initial state and the set threshold voltage required to switch the device to the strong (i.e. highest conductance) ON state. (c)–(f) Example of  $Q^* \leftarrow P$  IMP  $Q$  operation with additional refresh step, in particular showing refresh operation for the partially switched device  $Q^*$  ((c), (d), and (f)), and negligible disturbance of the device  $Q^*$  OFF state on (e).

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