Fabrication, CMOS integration and applications of non-volatile 3D metal oxide crossbars

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***Abstract*—As the rapid progress of memristor technology continues, multi-layer stacking of these crossbars is needed in order to maximize the use of vertical space and achieve the required density. This work is focused on designing and building three-dimensional monolithically integrated memristive crossbars, both standalone and onto CMOS chips. Firstly, we reported the first three-dimensional monolithic integration of two 10x10 TiO_{2-x}-based passive crossbars with good yield and less than 175°C temperature budget suitable for CMOS integration. As a second step, we demonstrated a hybrid 3D circuit based on the CMOL architecture with 2 layers of memristive crossbars monolithically integrated on a pre-fabricated CMOS substrate. The integrated crossbars were operated through the underlying CMOS circuitry and showed stable multi-state operation. Such crossbars are an important step towards energy-efficient hardware implementations of neuromorphic circuits, highly dense non-volatile memories with in-memory computing capabilities and for hardware implemented security primitives.**

Keywords—Three-dimensional (3D), crossbar, metal-oxide, analog, material implication, CMOS integration, security primitives

I. Introduction

The 3D "CMOL" (CMOS+molecular devices) architecture [1] implemented using resistive switches is a promising candidate for energy-efficient hardware implementations of neuromorphic circuits and dense non-volatile memories. The thermal budget, yield and uniformity have to be considered during the fabrication of such hybrid multi-stack systems. The memristors should have tight switching variations to achieve high performance circuits. There have been demonstrations of multi-layer crossbar circuits [2-3], but targeted towards digital memories and showing limited characterization statistics. Sidewall vertical integration is a cost-effective stacking solution [4-5], but it has been shown so far only for small linear arrays, not crossbars, and is not suitable for CMOL.

There have been reports where memristors were fabricated between CMOS metal layers or onto CMOS chips [6-8], but they include limited discussions on the quality of the interface between the CMOS chip and the layers of resistive switches. Recently, in-memory computation capability was shown in 3D vertical resistive memory devices monolithically integrated with FinFET selectors [6]. However, successful demonstrations of CMOL circuits are still missing.

II. Experimental Results

This work is focused on designing and building 3D monolithically integrated memristive crossbars, both standalone and onto CMOS chips, and further using them for prototyping promising applications. Firstly, we reported a 3D monolithic back-end-of-line integration of two Pt/Al_2O_3/TiO_{2-x}/TiN/Pt -based passive crossbars with shared middle electrode (Fig. 1a-c) [9]. A planarization step performed before the deposition of the second crossbar led to 74% yield across 4" wafer and allowed successful forming and tuning of all 200 devices in the demonstrated crossbar circuit. The stacked 3D crossbars were used as compact and highly non-linear programmable analog instances to implement PUF security primitives. The demonstrated PUF exhibits almost ideal randomness.

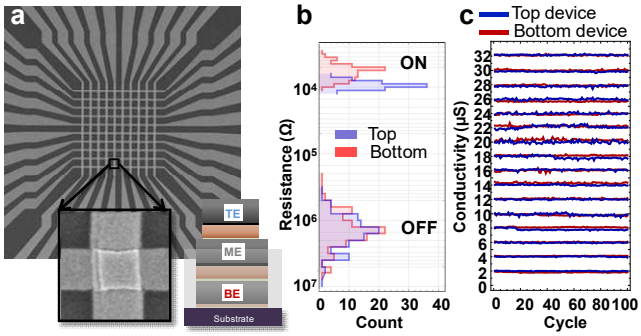

Fig. 1. Standalone 3D crossbars (a) Top-view SEM image of the 3D stacked crossbar with cross-sectional schematic (b) Cumulative histogram for the devices' ON and OFF state conductances, measured at 0.3 V (c) Tuning results to 16 different conductive states -from 2 μS to 32 μS- for top and bottom devices (d-h) Fabrication and operation of a 3D CMOL crossbar.

The tunable resistance of memristors is also suitable for stateful logic, but the device variations pose challenges for conditional switching over many switching cycles. We demonstrated an optimized circuit configuration [10] and proved its reliability by experimentally showing a multi-cycle multi-gate material implication logic operation within a 3D passive stack of monolithically integrated memristors with no selectors. Three dimensional data manipulation can enable extremely compact and high-throughput in memory computing. This approach could offer a solution for the

Feynman Grand Challenge of implementing an 8-bit adder in 50x50x50nm.

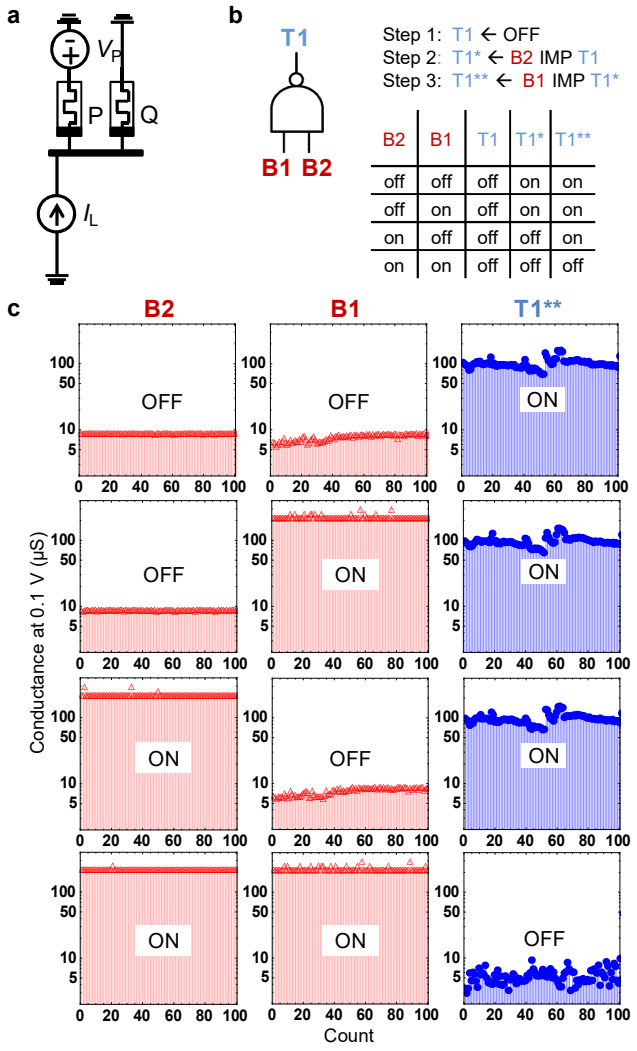

Fig. 2. Multi-cycle operation of three dimensional NAND gate implemented using memristive-based implication logic (a) Proposed optimized circuit for implication logic (b) Three dimensional NAND gate symbol and implementation steps (c) Experimental data showing 100 cycles of operation.

As a second step, we demonstrated a hybrid 3D circuit based on the CMOL (CMOS + "Molecular") architecture with two (2) layers of memristive crossbars monolithically integrated on a pre-fabricated CMOS substrate (Fig. d-g) [11]. The layers of memristive crossbars were added via post processing of the 5mm x 5mm CMOS chip, firstly by planarizing the chip using chemical mechanical polishing to create a suitable smooth surface, then etching 4μm x 4 μm vias to connect electrically the CMOS chip with the memristive lines. Reactive sputtered Al_2O_3/TiO_{2-x} were used as active layer for both of the memristive stacks. The two crossbars can be fully operated by the underlying CMOS circuitry and exhibit analog switching behavior with controlled tunability and stable multi-level operation. The memristors have an entirely passive operation and no selector was used in the design. Dot-product operations were performed to demonstrate the applicability of 3D CMOL circuits as a multiply-add engine.

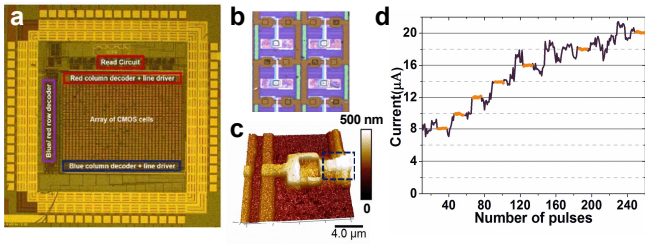

Fig. 3. Hybrid 3D circuit for CMOL architecture, based on a (a) foundry processed CMOS chip with (b) arrays of CMOS cells used for accessing the (c) two layers of memristive devices; (d) Typical pulsed set/reset switching characteristics.

Conclusions

In summary, we have experimentally demonstrated monolithically integrated passive memristive crossbars, standalone and onto CMOS circuitry. Planarization based on chemical mechanical polishing and dry etch-back was used to provide a smooth surface for stacking memristive crossbars. The stand-alone 3D crossbars showed good uniformity and were used for the implementation of PUF security primitives with almost ideal randomness. An optimized circuit for implication logic implemented using stacked memristive devices showed reliable multi-cycle operation. The 3D memristive crossbars monolithically integrated onto CMOS circuitry implemented a multiply-add engine as the first 3D CMOL hybrid circuit demonstration.

References

[1] K. K. Likharev, "Hybrid CMOS/nanoelectronic circuits: Opportunities and challenges", J. Nanoelectronics and Optoelectronics, vol. 3, pp. 203-230, 2008.

[2] T.-Y. Liu et al., "A 130.7 mm2 2-Layer 32-Gb ReRAM memory device in 24-nm technology", IEEE Journal Solid-State Circuits, 49 (1), pp. 140-153, 2014.

[3] M.J. Lee et al. "2-stack 1D-1R cross-point structure with oxide diodes as switch elements for high density resistance RAM applications" IEDM, pp.771-774, 2007.

[4] S. Yu et al., "HfOx-based vertical resistive switching random access memory suitable for bit-cost-effective three-dimensional cross-point architecture", ACS Nano, vol. 7, pp. 2320-2325, 2013.

[5] P.Y. Chen, Z. Li, S. Yu, "Design tradeoffs of vertical RRAM-based 3-D cross-point array", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, PP (99), 2016.

[6] H. Li et al. "Four-layer 3D vertical RRAM integrated with FinFET as a versatile computing unit for brain-inspired cognitive information processing", IEEE Symposium on VLSI Technology, 2016.

[7] K. H. Kim et. al. "A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications", Nano Letters, vol. 12 (1), pp. 389-395, 2011.

[8] Q. Xia et al. Memristor–CMOS Hybrid Integrated Circuits for Reconfigurable Logic, Nano lett. 9, 3640-3645, 2009.

[9] G.C. Adam et al. "Highly-uniform multi-layer ReRAM crossbar circuits." European Solid-State Device Research Conference (ESSDERC), pp. 436-439, 2016.

[10] G.C. Adam et al. "Optimized stateful material implication logic for three-dimensional data manipulation." Nano Research 9, no. 12, pp. 3914-3923, 2016

[11] B. Chakrabarti et al. “A multiply-add engine with monolithically integrated 3D memristor crossbar/CMOS hybrid circuit”, Scientific Reports, 2017, 7, 42429.