Toward an Empirical Compact Model for Crossbar Integrated Metal-Oxide Memristors

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The development of large ReRAM circuits depends on the availability of predictive models of their memristive cells. If progress has been made in understanding the physics of such nanodevices in the last 10 years, developing compact models, required by EDA simulation tools, that are accurate but yet fast to simulate has proven to still remain a significant challenge.

We introduce a comprehensive model, and its conception workflow, for metal-oxide memristors integrated in crossbars, named “MEMPHIS” (for MEMristor PHenomenologIcal Simulator). To stay computationally light, this empirical model avoids using coupled differential equations like most of the other compact models available in the literature. Instead it relies on two explicit equations, a static and a dynamic one, that are computationally inexpensive and suitable for SPICE simulations. In order to capture the effect of the device variations, both equations are fitted on a large amount of experimental data, which come from measurements on several hundreds of devices, that were fabricated in our laboratory.

The static equation describes the I-V curve of the devices at low bias voltage, i.e. under non-disturbing memory state conditions, by the sum of three components that represent the average behavior of the crossbar devices, the device-to-device variations, as well as the temporal noise. Those components are expressed as simple functions of the applied voltage, the device memory state and the ambient temperature. The dynamic equation describes how the memory state of a device is modified when applying a large voltage pulse. This equation depends also on the duration of the programming pulse and on the initial memory state of the device. Similarly to the static equation, two components are summed together: one for the average device behavior and another one for describing the device-to-device effects.

We apply this model to crossbar arrays of TiO2-based memristive devices and show by means of validation results that it has a good predictive power. As the model has been obtained for a representative device structure, following a quite general workflow, we expect it to be applicable to other nonvolatile memory technologies.

Finally, we present use cases of the model. A first possible example comes from the framework of vector-matrix multiplication, which is a critical operation for various tasks and systems like computer vision or hardware (rate-based) neural networks. We highlight how the comprehensive aspect of the model allows to identify the most challenging issues, especially during inference, that are due to various parasitic elements, e.g. the line resistance, the non-linearity of the memory devices, their drift or their noise. This study also shed light on the trade-off that have to be made when scaling the crossbar dimensions regarding those issues. A second application that we may explore is the field of spiking neural networks. By leveraging the predictive power of our model when it comes to device variations, we can get insights on how to deal with the imperfections of the memristive nanodevices used as artificial synapses. This is especially useful when setting up small scale demonstrators of hardware spiking neural networks, where simulations can be of high value to develop mitigating strategies against such issues.

In conclusion, we introduce a computationally-friendly empirical model for metal-oxide memristors, that follows a general workflow, which may be extended beyond the devices that were available to us. We then show how such a model can be useful to perform realistic simulations of memristor-based circuits in the field of mixed-signal neuromorphic networks, which make use of the analog behavior of the studied devices but can be sensitive to their nonidealities. These results will contribute to opening a way towards highly energy-efficient unconventional computing systems that rely on innovative nonvolatile memory devices.