MEMRISTIVE DEVICES

Tightening grip

Engineering channels for ion transport in a SiGe solid-state electrolyte layer allows one to significantly decrease the spatial and temporal variations of the electrical characteristics in resistive switching memories.

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Despite very appealing density and performance prospects of resistive switching memories (also called memristors or memristive devices), the fluctuations in current–voltage (I–V) characteristics that can be found in an array of nominally identical memristors are still by far the most challenging obstacle between their widespread deployment in memory and computing applications. Writing in *Nature Materials*, Shinhyun Choi and colleagues[1] report a significant milestone towards addressing this challenge — they realized devices based on a Ag/SiGe/p-Si material stack having customized channels for the formation of conductive ionic bridges, which feature electrical properties with high spatial and temporal uniformity.

In the simplest case, an ionic memristor consists of a thin insulating film sandwiched between two conductive electrodes (Fig. 1a). Application of an electrical stress across the electrodes changes the thin film's conductance, resulting in a pinched hysteresis I–V loop when a sequence of positive and negative voltage sweeps is applied (Fig. 1b). The conductance modulation is due to drift of ions in the insulating material, which may be anions that are intrinsic to the insulating material (such as charged oxygen vacancies in transition-metal oxides[2]) or cations supplied by an active electrode (Fig. 1a). In the latter memristors, known as conductive-bridge devices[3], a strong electric field triggers redox reaction at the interface and forces charged ions to move in an ion-conductive solid-state electrolyte eventually forming a conductive filament that bridges the insulating matrix. By changing the polarity of the field, the process is reversed. Both types of ionic memristors have been very actively investigated in academia and industry in the past decade due to their potential 'universal memory' characteristics. These include fast (sub-nanosecond) switching combined with long (year-scale) memory retention, scalability of the device size below 10 nm, and suitability for monolithic three-dimensional integration[2–4]. Moreover, the conductance of many memristors can be changed gradually, which is essential for many computing applications[4].

The ionic memory mechanism, however, comes with several distinct challenges. First, the reported cycling endurance — the average number of times the devices in integrated circuits can be reliably cycled between on and off states — has been so far much smaller compared to that of conventional volatile memories and some emerging nonvolatile memories based on purely electronic switching mechanisms (such as magnetic memories). The primary causes are the higher energy required to move ions[5], which induces permanent changes in the device stack, and the loss of mobile ions from the active region due to gradual lateral diffusion[2].

The most critical challenge, at least for neuromorphic and other analogue computing applications[4], has been the large device-to-device (spatial) and cycle-to-cycle (temporal) variations in memristors' I–V characteristics, most importantly in the effective switching threshold voltages (insets in Fig. 1b). The cause of such variations is closely related to the filamentary switching mechanism, which is typical for the majority of the ionic memristors. Most typically, the conductive filaments are first created during the so-called forming step, which is a one-time application of larger electrical stress[2–4]. In metal-oxide memristors, the forming step is initiated by electrical breakdown that creates extremely hot regions, which then serves as a preferential path for ion transport, leading to the formation of the filament. Naturally, breakdown runaway process is hard to control and variations in the structure and composition of the formed filaments are behind poor device uniformity[6]. In conductive-bridge memristors with homogeneous thin-film structure, the formed filaments would typically have dendrite-like stochastic shapes, which cause device-to-device and cycle-to-cycle variations[3].

A strategy explored to improve uniformity is to constrict the electrical and ionic currents during forming. This can be achieved with specifically engineered electrodes with protrusions or wedge shapes[7], or creating special opening

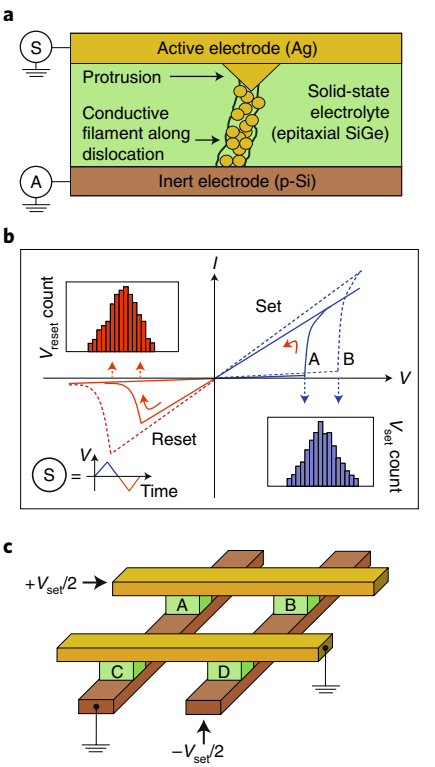

Fig. 1 | Switching threshold variations in memristors. a, Conductive-bridge memristors with engineered protrusion. **b**, Typical I–V hysteretic curve, shown for simplicity for a linear device, resulting from the application of a symmetric voltage sweep (lower bottom inset). The inset histograms show variations in the switching voltages at which conductance changes. (Note that there is no sharp threshold for switching and, in principle, the thresholds weakly depend on the voltage ramp rate. In that sense, the thresholds are rather 'effective' voltage values which are representative of the intended operating conditions.) **c**, A four-device passive crossbar circuit with integrated memristors at each cross-point. The applied voltages show specific example of the 'half-biasing' technique used to increase the conductance (setting) of the device B.

for ion transport[8]. Choi and colleagues demonstrated a more advanced approach for controlling filaments in Ag/SiGe/p-Si conductive bridge devices. SiGe material was epitaxially grown with vertically aligned high-density (10^{11} cm^{-2}) threading dislocations (Fig. 1a). The upper end of the dislocations was widened via selective etching to effectively create a protrusion in the top electrode. As a result, conductive filaments were observed to form along the dislocations that acted as preferential diffusion paths for Ag ions. Additionally, due to low solid solubility in SiGe, Ag diffusion into the bulk was negligible. The very fine control over the filament formation ultimately resulted in highly uniform device *I*–*V* characteristics.

The importance of uniformity in devices' *I*–*V*s can be illustrated by considering the protocol typically used to program memristors to specific states. In the most prospective 'passive' crossbar circuits (Fig. 1c), the memristor conductance is gradually tuned to the desired values with a sequence of write steps, in which half of a large-amplitude voltage pulse (V_{set}) is applied to each of the electrodes of the selected device (B), while all other electrodes are grounded[4,7]. The switching threshold variations must be tight enough to ensure that the $V_{set}/2$ pulse does not alter the conductance of the 'half-selected' devices A and C.

The discussed tuning operation is routinely performed in the simplest type of artificial neural networks trained by ex situ methods, where conductances of the memristive devices, playing the role of artificial synapses, have to be programmed according to the pre-calculated synaptic weights[7]. Variation requirements are much stricter for more advanced computing application of memristors, such as neural network relying on real-time hardware-implemented ('on-line') training[1,7], and in-memory computing[4,9]. In these applications the same fixed write voltages must be used for all devices, which is naturally less tolerable to variation approach compared to flexible tuning algorithm. In this context, the reported uniform *I*–*V* characteristics by Choi and colleagues — ~5% standard deviation in set threshold voltages on a batch of 500 memristors — are especially important.

An evident drawback of the demonstrated approach is, however, the high temperature budget required for heteroepitaxial SiGe growth, which is incompatible with complementary metal-oxide semiconductor (CMOS) fabrication technology. Indeed, memristor-based computing relies heavily on standard CMOS circuits, hence high-throughput monolithic integration between CMOS and memristive devices is necessary for high-performance and energy-efficient implementations. Additionally, the reported device characteristics must be confirmed for memristors down to the nanoscale, which are required for high-density circuits. Although further work will be needed to find a solution to these issues, the work by Choi and co-authors, along with other recent breakthroughs[10], already presents much-needed evidence that variations problems can be resolved with smart engineering. ❐

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