
COPEN
wireless oscilloscope

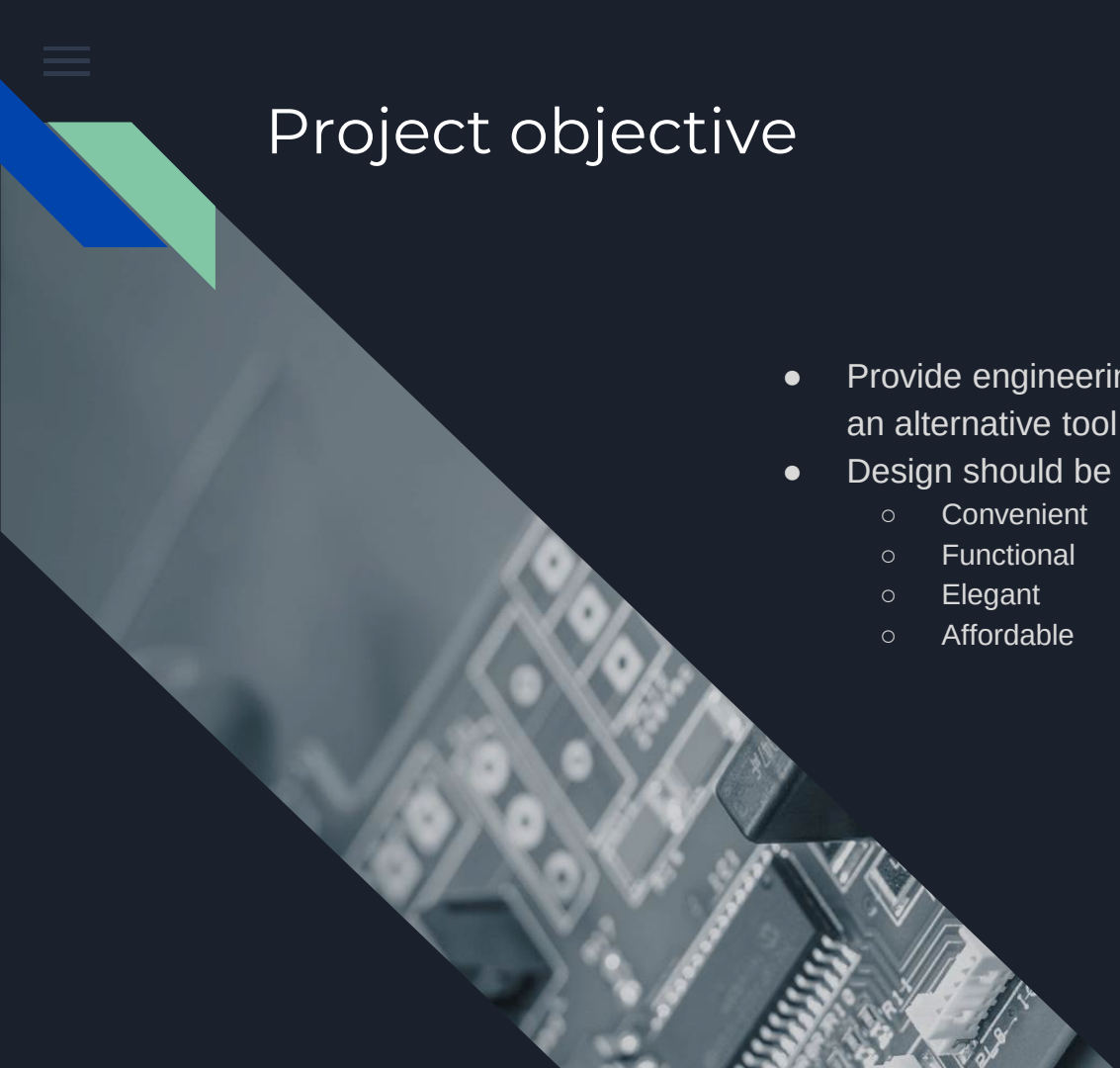
Team

- Byron Aguilar
  - AFE Design
  - Team Leader
- Boning Dong
  - FPGA Design
  - Subsystem Interface Design
- Cesar Gonzalez
  - AFE Design
  - Power Management

Wireless Oscilloscope

- Appearance of a pen,
  - Easy use with one hand
- Measure arbitrary voltage waveforms
  - Up to 50Vpp
  - Up to 20MHz Bandwidth
- Data Transmitted via WiFi to PC
- Software will provide functionalities of a regular bench-top oscilloscope

Project objective



- Provide engineering hobbyists and students with an alternative tool for their study.
- Design should be
  - Convenient
  - Functional
  - Elegant
  - Affordable

Design Breakdown

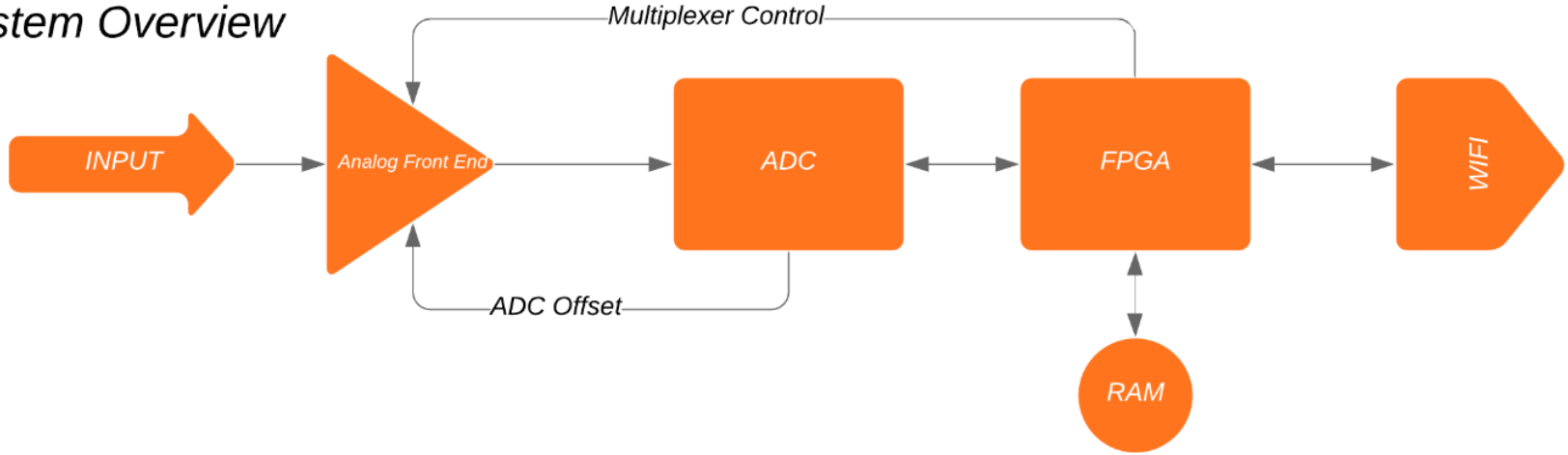
01 Analog Front End Design: Handle initial input and convert it to acceptable differential voltages that will be fed into the ADC

02 ADC/FPGA/Memory: ADC samples differential signal and transmits data to FPGA. Data is stored and then sent to Wi-Fi module

03 Software Programming: Receives data and reconstructs the signal. Displays signal

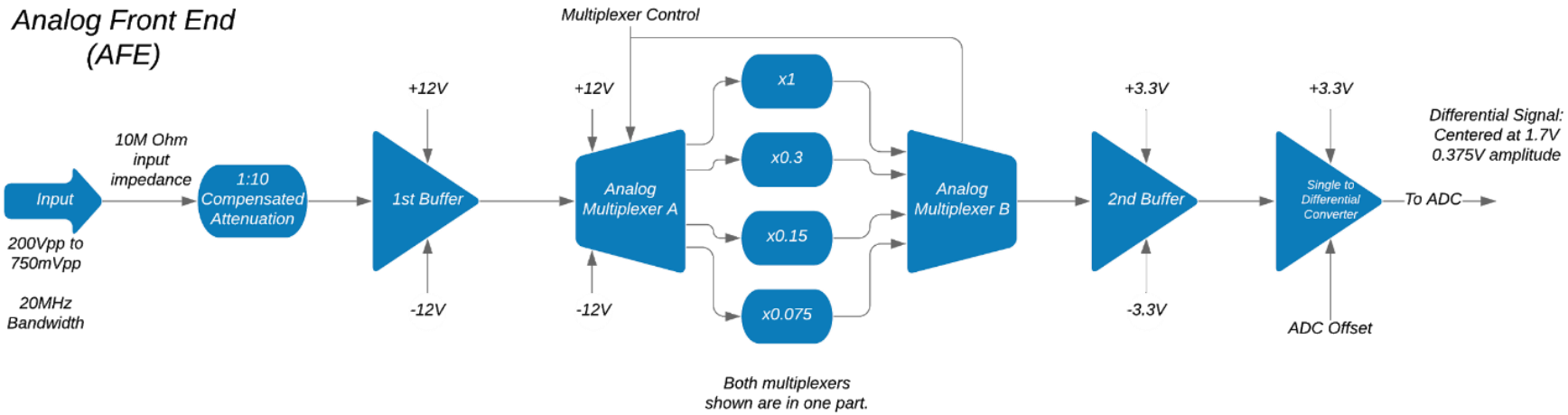
Block Diagram

System Overview

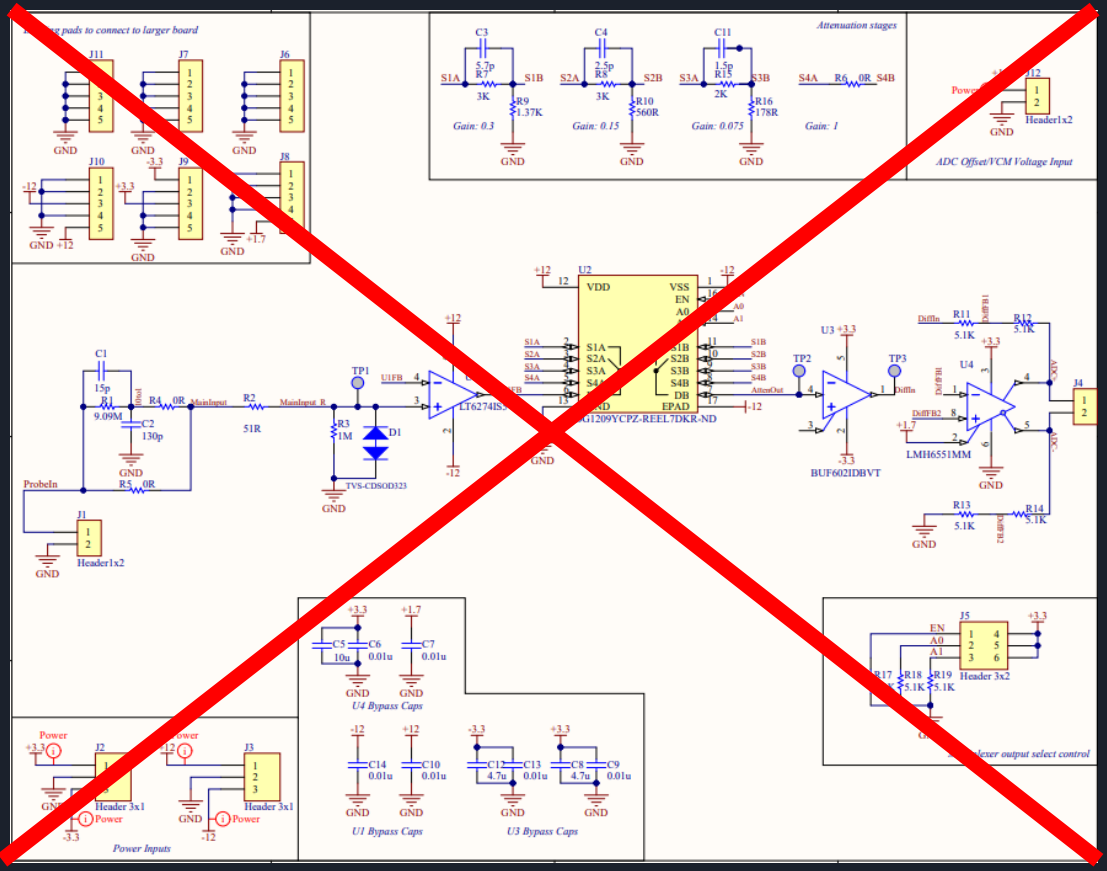


AFE Design Requirements

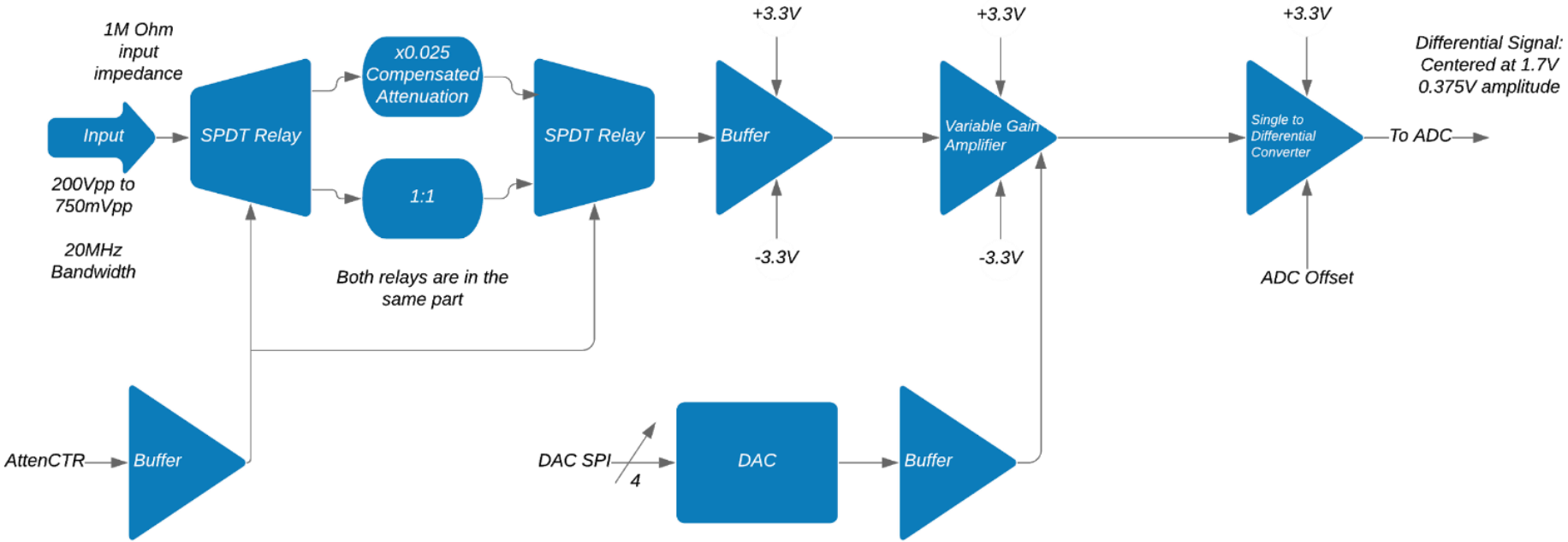
- Input can be almost anything
  - Protection must be included against too high voltages
- Ideal AFE should not distort or modify the general form of the original signal
- AFE should be able to scale an input to the best possible voltage range for the ADC


Analog Front End (AFE)
Multiplexer Control
+12V
+12V
+3.3V
+3.3V
Differential Signal: Centered at 1.7V 0.375V amplitude
10M Ohm input impedance
Input
1:10 Compensated Attenuation
1st Buffer
Analog Multiplexer A
x1
x0.3
x0.15
x0.075
Analog Multiplexer B
2nd Buffer
Single to Differential Converter
To ADC
200Vpp to 750mVpp
20MHz Bandwidth
-12V
-12V
-3.3V
ADC Offset
Both multiplexers shown are in one part.

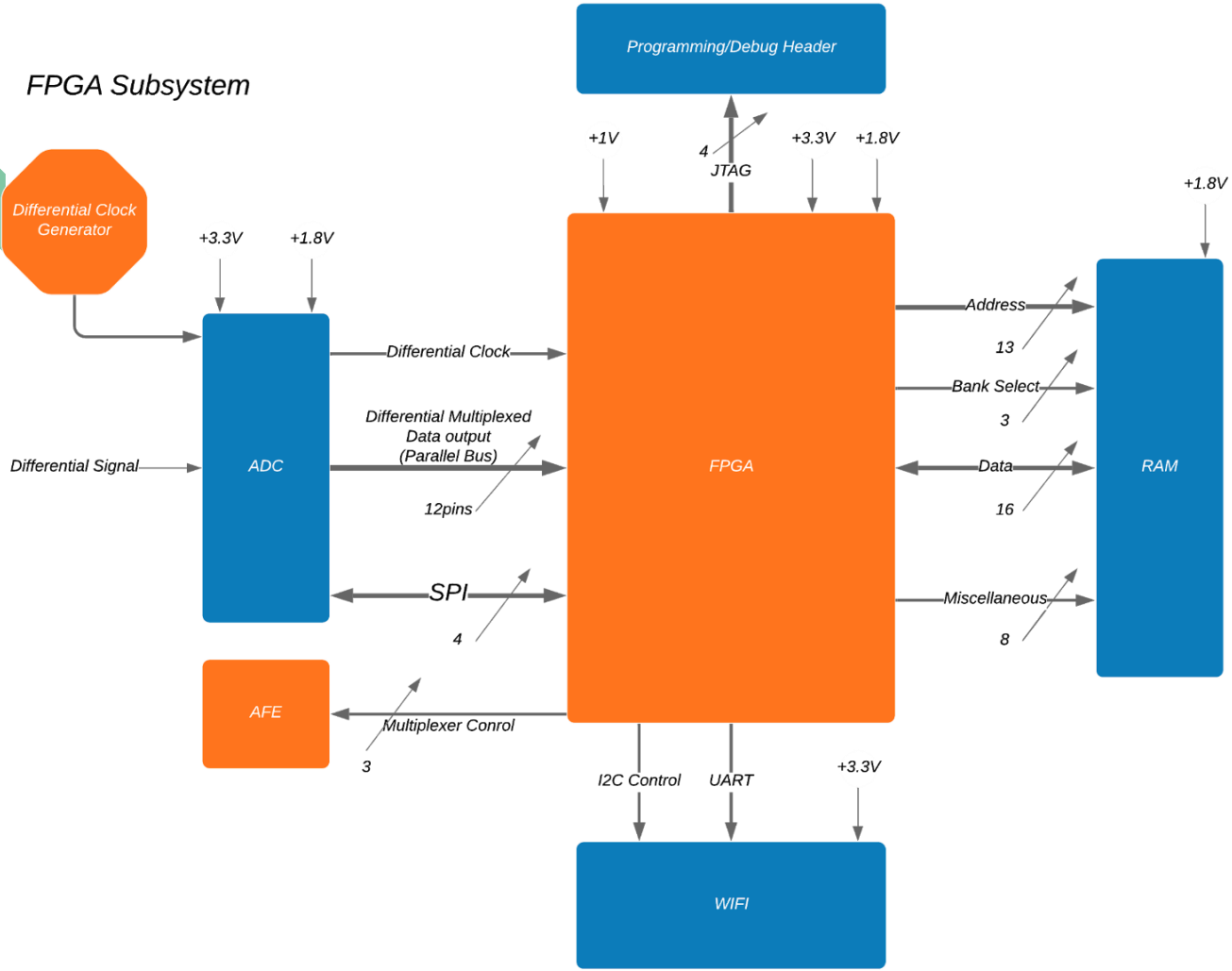
AFE Schematic



Analog Front End (AFE)

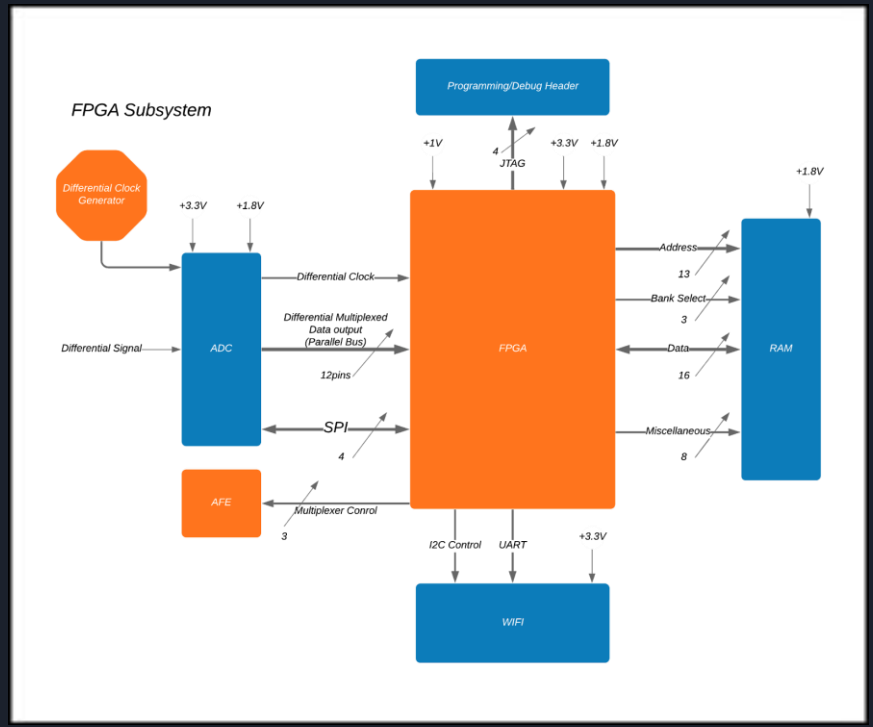


FPGA Subsystem



FPGA and Subsystem Interfaces

- Understand FPGA interface
  - FPGA Architecture
  - IO Standards
  - Resources Evaluation
- Under all subsystem interface
  - DDR2 Memory
  - ADC
  - JTAG
  - WIFI (ongoing)
  - MCU (ongoing)



1. FPGA Interface

a. FPGA Architecture

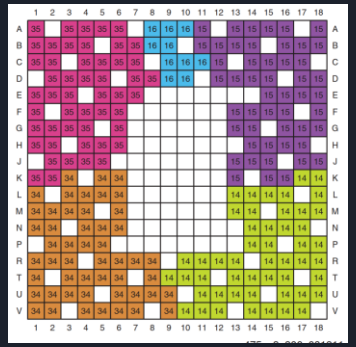
- IOs within the same bank are powered by the same power source.
- Some interface such as memory interface cannot cross banks.

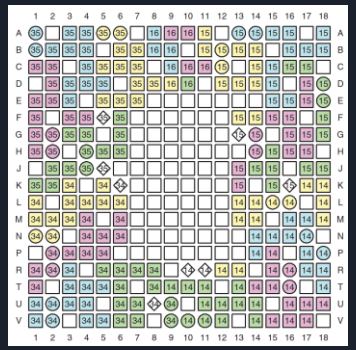
a. IO Standards

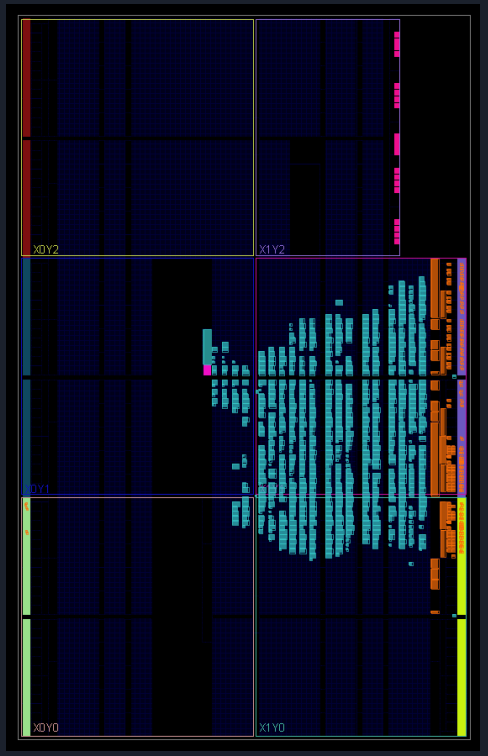
- LVCMOS: Low Voltage CMOS
- LVDS: Low Voltage Differential Signals
- SSTL: Stub Series Terminated Logic

a. FPGA Resources Evaluation

- Implemented a memory controller to check the resources usage.







2. Subsystem Interface

a. DDR2 Memory

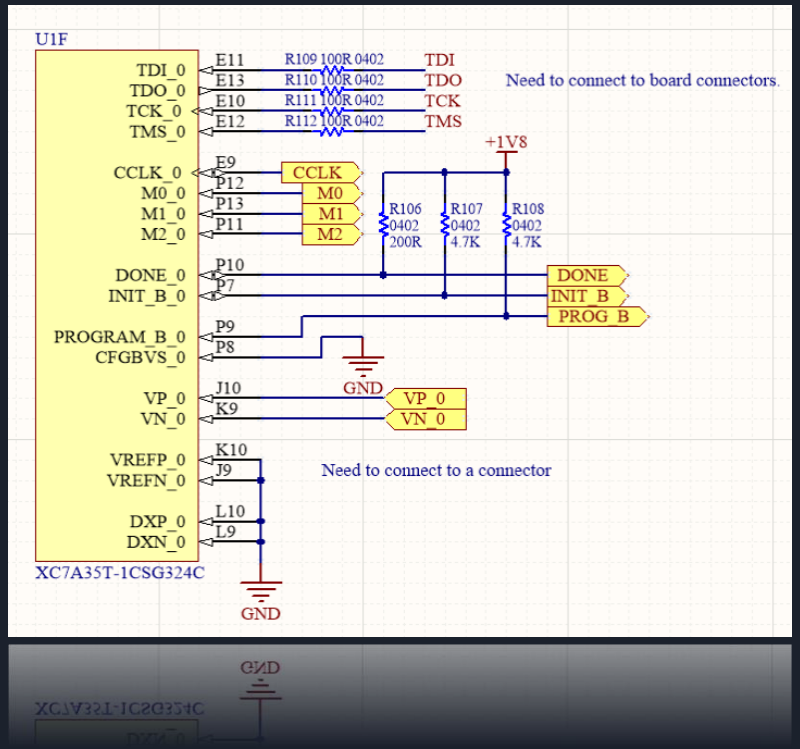
- SSTL_18 IO Standard
- Controlled using Vivado MIG IP Core.
- [PCB] Requires impedance & length matching

a. ADC

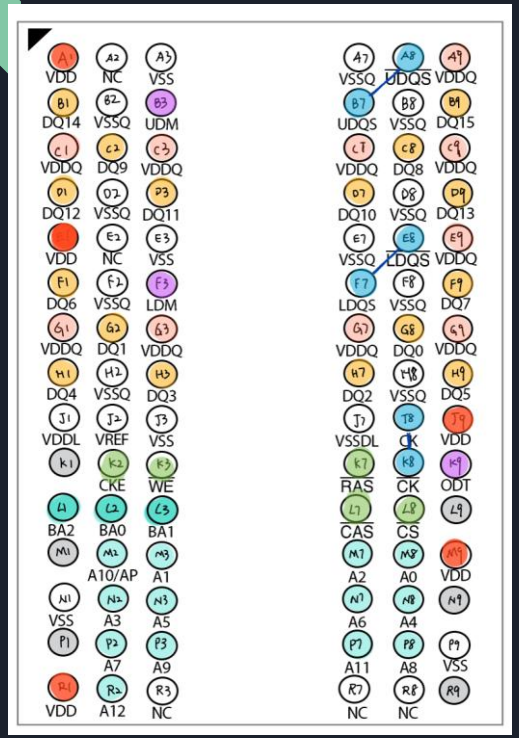
- Using LVDS_18 IO Standard
- SSTL: Stub Series Terminated Logic
- [PCB] Requires differential pairs.

a. JTAG

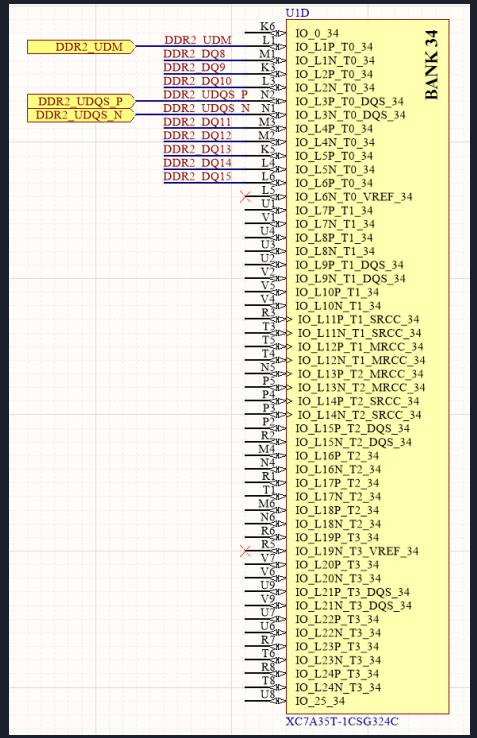
- Pin definition has been given out.
- May need serial resistors for voltage conversion.

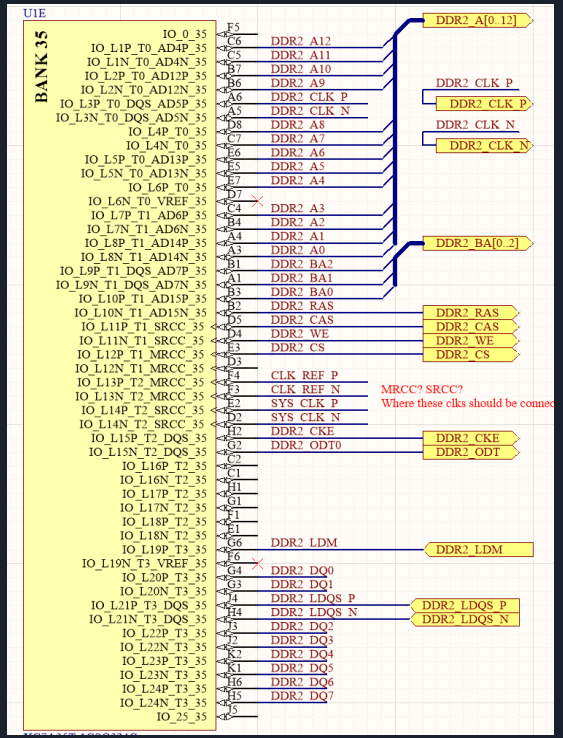


Schematics - DDR2 Memory



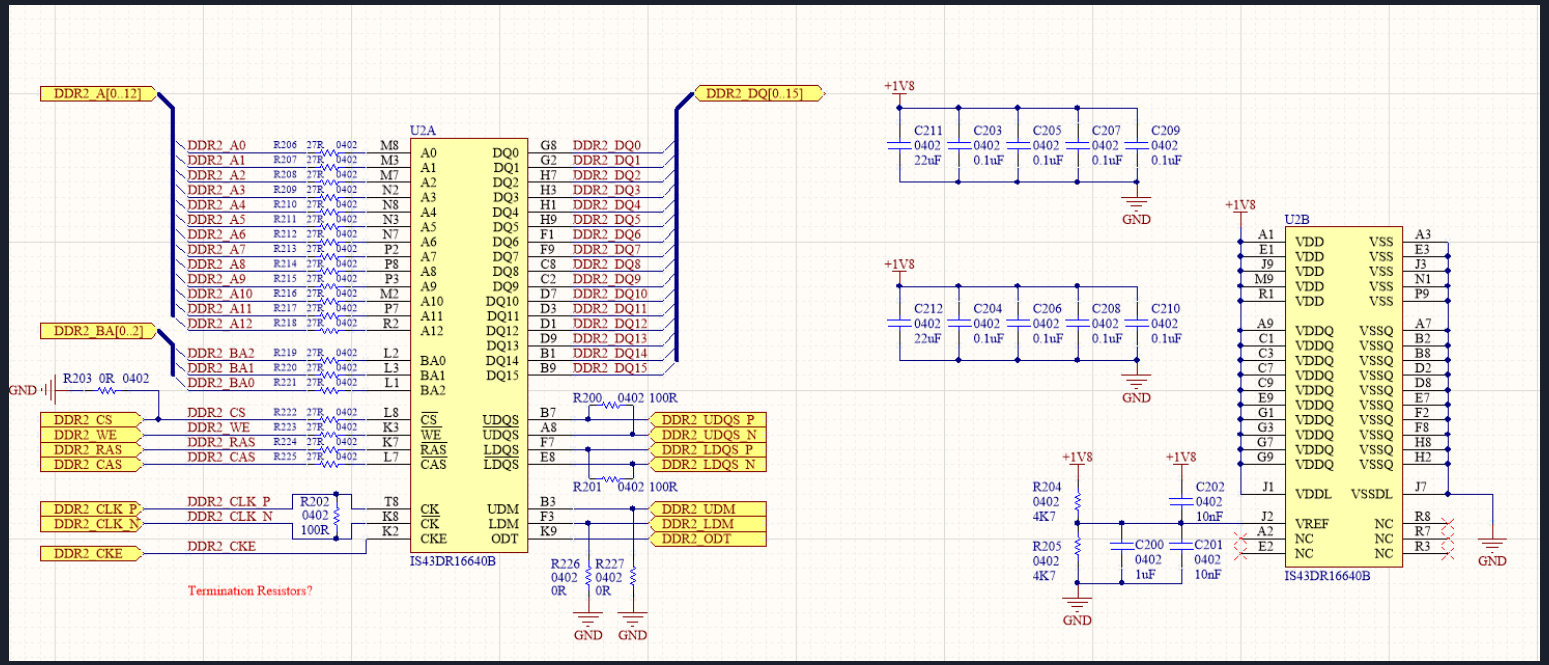
Package Pinout





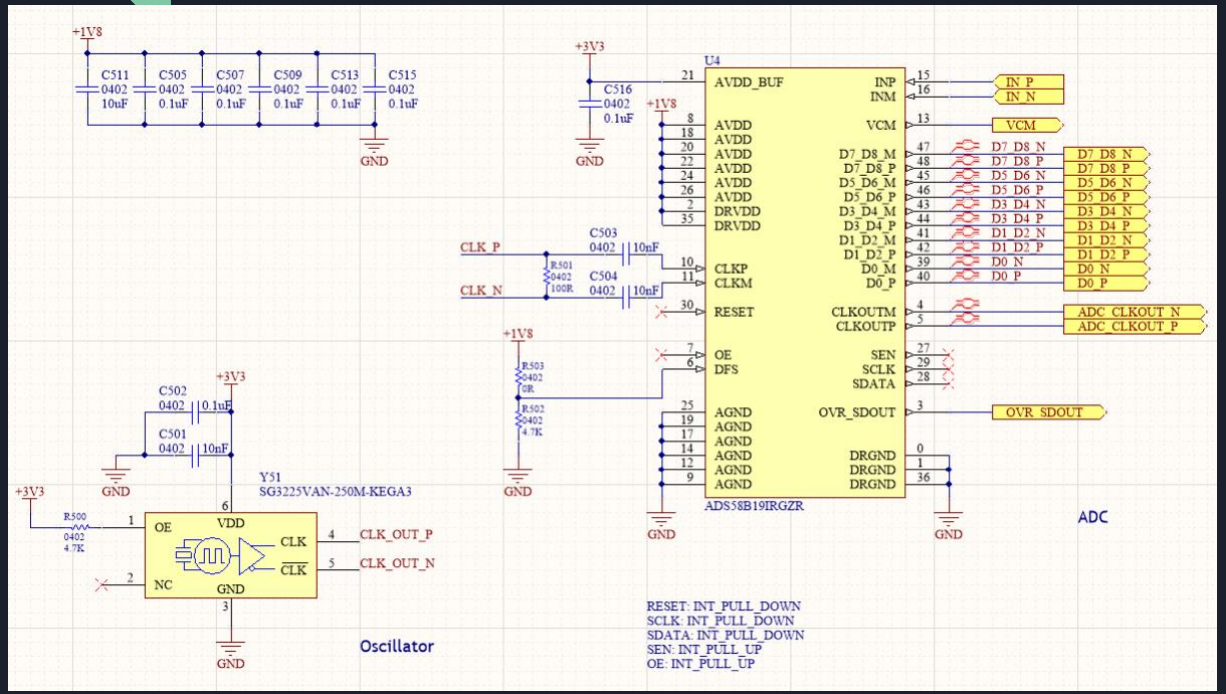
FPGA Bank 34 & 35 IO assignments for the RAM

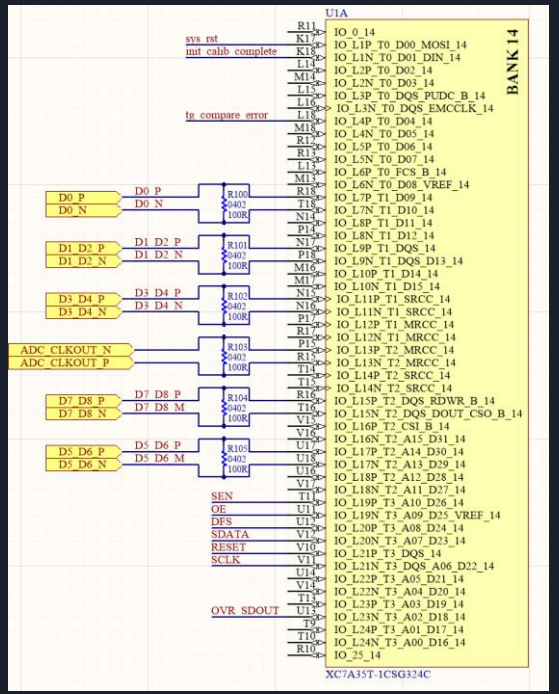
Schematics - DDR2 Memory



DDR2 Memory & Memory Power Supply

Schematics - ADC

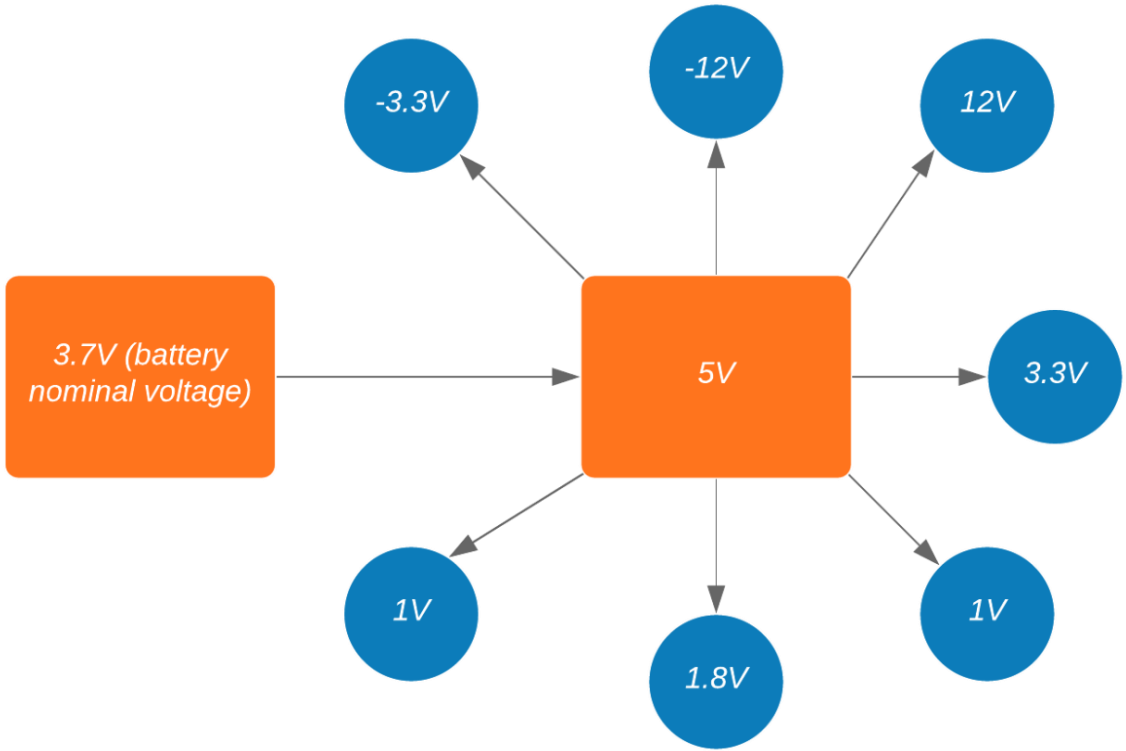




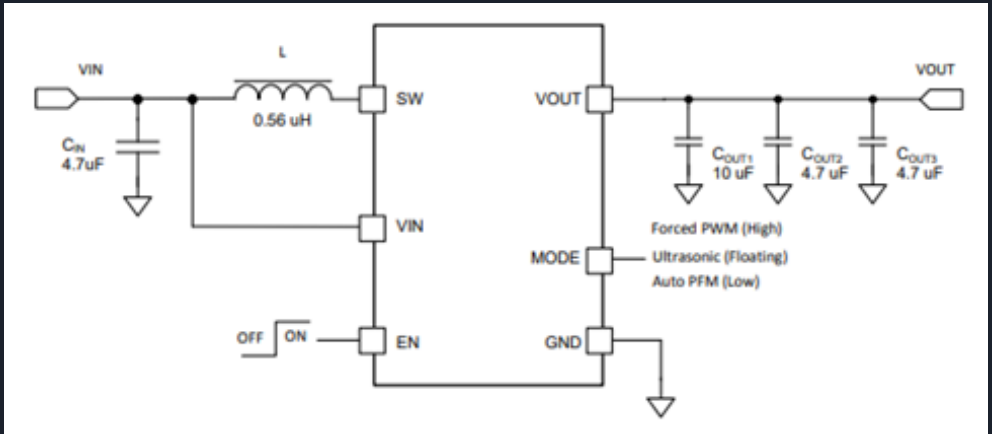
Clock Source & ADC

FPGA Bank 14 IO assignments for the RAM

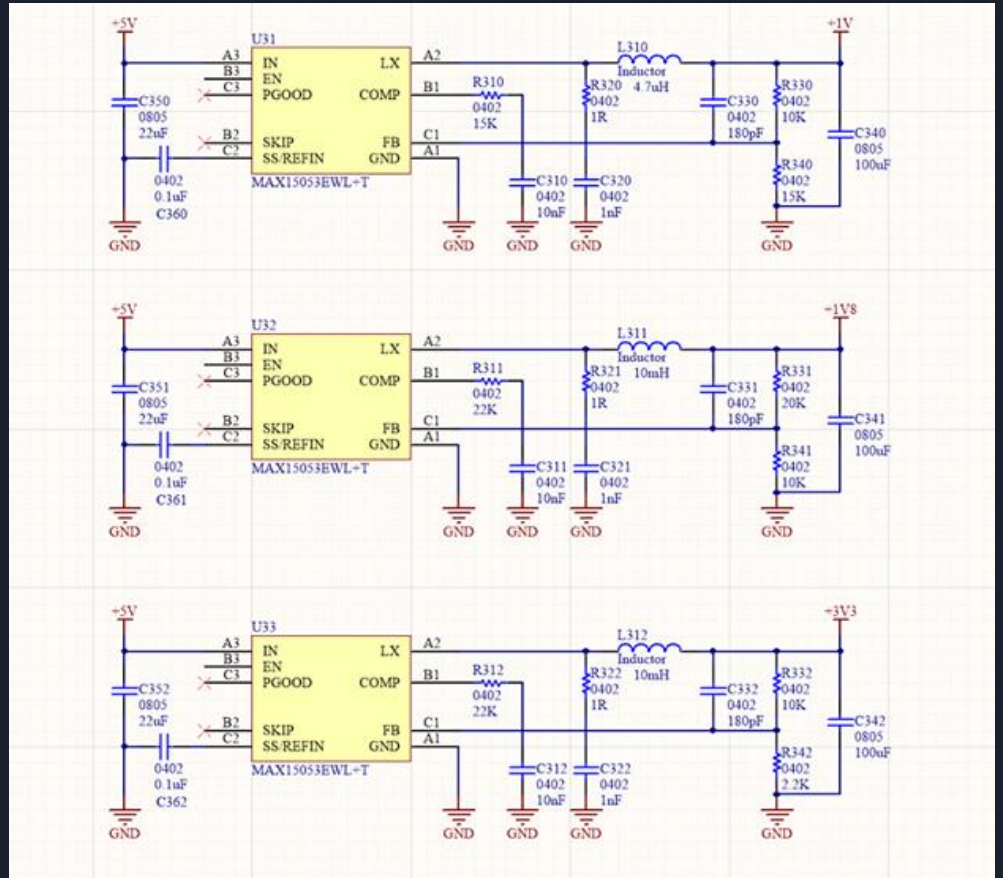
Power Tree



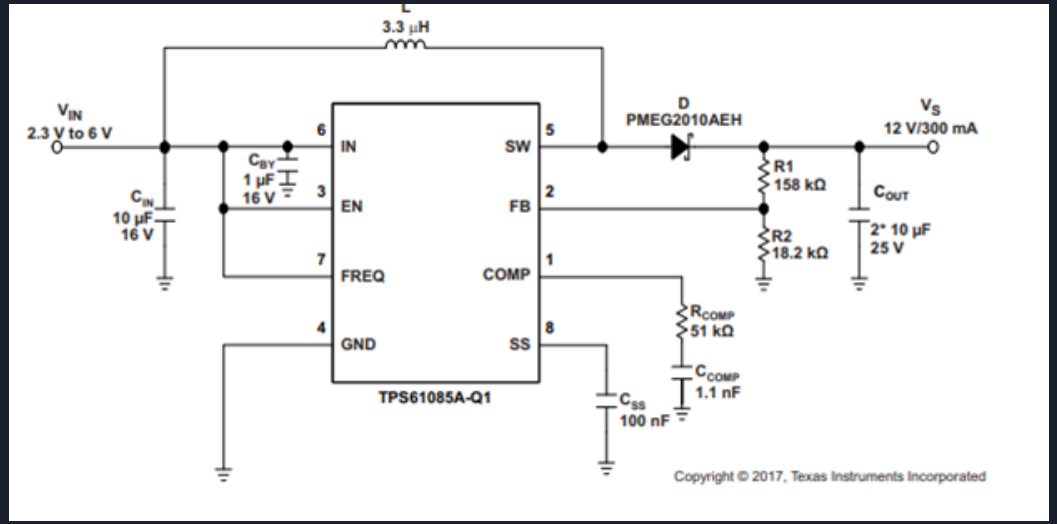
3.7V → 5V Boost Converter



5V → 1V, 1.8V, 3.3V Buck Converters



5V → 12V Boost Converter



5V → -12V Inverting Converter

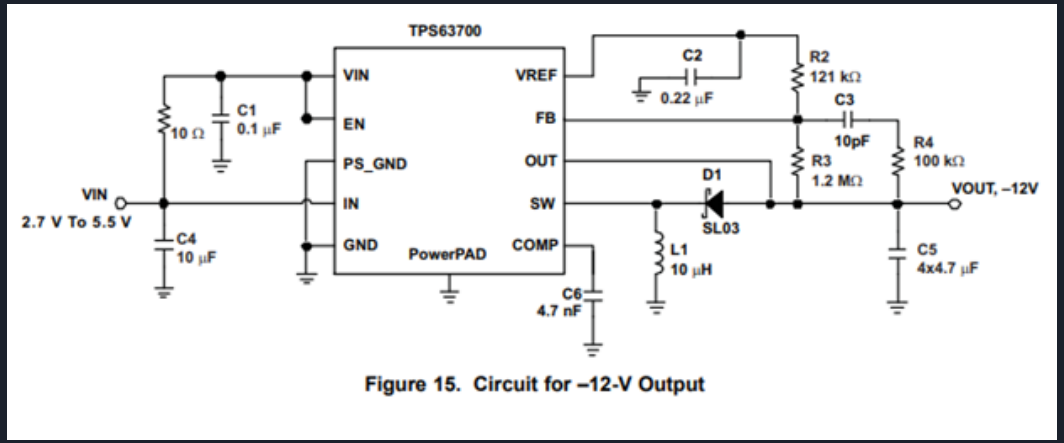
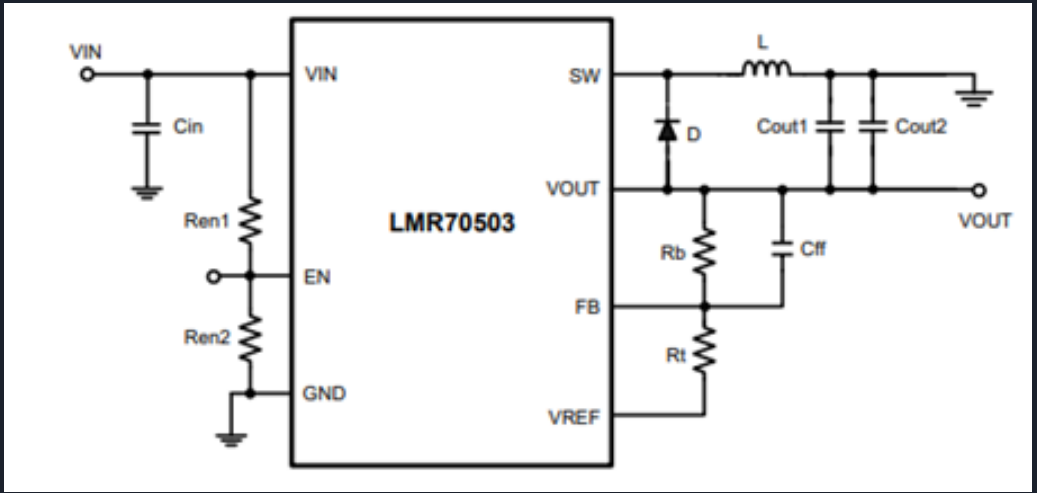


Figure 15. Circuit for –12-V Output

5V → -3.3V Buck Boost Inverting Converter



Goals

- Create main test and coding platform which combines all subsystem modules
  - Currently we are designing each subsystem PCB separately and we will combine them into one at the end of this quarter
- Begin testing of overall system
- Begin planning of software architecture

Current Progress

- Reworking AFE design
- Beginning layout work for the FPGA Subsystem
- Beginning main schematic for main system board

Acknowledgements

Thanks to:

- Professor Yoga
- Professor Brewer
- Adi
- Kyle

Any Questions?